User's Manual

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MSC8102ADS

User's Manual

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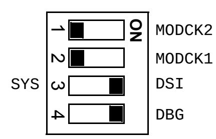
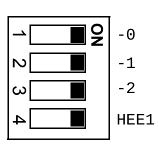
Section 1 Getting Started

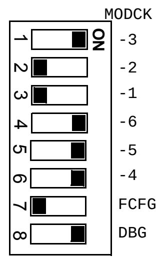
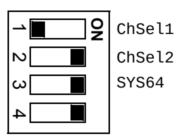
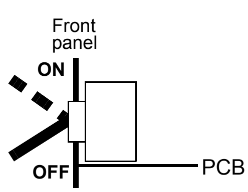
This Quick Start Guide shows MSC8102ADS board switches and jumpers in their default positions.

1.1 Switches

ADS Dual-In-Line Package (DIP) Switches are listed and described in *Table 1-1*. The switches and jumpers featured in this chapter are shown with their factory-default positions. ADS board LED's are also detailed.

Table 1-1 The ADS Switches

Designator & Purpose	Type	Description
SW4 Slave Configuration Control (MSC8102)	 CFG-S Ctrl	**SW4.1-SW4.2** set the MODCK1,2 of MSC8102 Slave to the PLL mode. When “ON”, the value is zero. When there is a clock-in frequency of 41.6MHz, the clock mode is set to 11. **SW4.3** (SYS <-> DSI) selects the power-up configuration source. MSC8101 Host is the configuration source when the DSI position is chosen. If SYS is selected then the MSC8102 Slave Flash is the configuration source. **SW4.4** While in DBG position, EE0 input is high at the time of Core reset. This allows the Cores to enter Debug mode immediately after negation of HRESETs. When not in the DBG position then, after reset, the Cores run freely. The Debug mode may be activated by toggling SW4/4. Factory settings: - MODCK1,2 are OFF - Config source from DSI - Debug mode after Slave’s Hard Reset
SW5 Software Option reading by MSC8101	 SW Opt	**SW5.1-SW5.3** set Software Option Bits 0-2 for SW flow control. When “ON”, the value is zero. **SW5.4** is used for Host EE1 pin control after Power-On-Reset. When “ON”, the value is zero. Reset Factory settings: - All bits set to ON

SW6 Host Configuration Control (MSC8101)	 CFG-H Ctrl	**SW6.1-SW6.6** set the MODCK1-6 of MSC8101 Host to the PLL mode. When “ON”, the value is zero. When there is a clock-in frequency of 55MHz, the clock mode is set to 57. **SW6.7** sets HCW1 source. When “ON” the source is Host Flash. If “OFF” then the source is a BCSR programmed value. **SW6.8** While in DBG position, EE0 input is high at the time of Core reset. This allows the Core to enter Debug mode immediately after negation of HRESETh. When not in the DBG position then, after reset, the Core runs freely. The Debug mode may be activated by toggling SW6/8. Reset Factory settings: -Clock Mode is 57 -HCW1 originates from BCSR -Debug Enable after Host Hard Reset
SW7 JTAG Chain Setting	 JTAG_CHAIN	**SW7.1-SW7.2** set the JTAG Chain configuration Bits 1-2. ChSel: 1 2 “ON” “ON” - Separate JTAG Access “OFF” “ON” - Short JTAG Chain “OFF” “OFF” - Long JTAG Chain **SW7.3** sets the Slave’s System Bus width. When “ON” the System Data Bus of the MSC8102 is 64-bit and the DSI bus is 32-bit. If “OFF” then the System Bus is 32-bit and the DSI bus is 64-bit. **SW7.4** Reserved. Reset Factory settings: -Short JTAG Chain -MSC8102 System Bus 64-bit The “JTAG Command Converter” plugs into the front of connector P14.
SW8 Power Switch		**SW8** When in the “ON” position power comes from an external 12V Power Supply via a P23 connector. When “OFF” the external power supply via P23 is disconnected. Consequently, when located in the CPCI backplane, the ADS is then powered by an internal power supply via cPCI connectors.

1.2 Jumpers

MSC8102ADS jumpers will be noted in the following sub-sections:

1.2.1 JP1 - External Power for CODEC

JP1 selects the source for the CODEC Power Rail. When a jumper is located between pins **1 - 2 of JP1** (Factory Set) then the CODEC feeds from the 3.3V plane of the ADS.

When a jumper is removed the 3.3V @ 200 mA external low-noise power supply may be connected to JP1 pins 2-3 as illustrated below in *Figure 1-1*

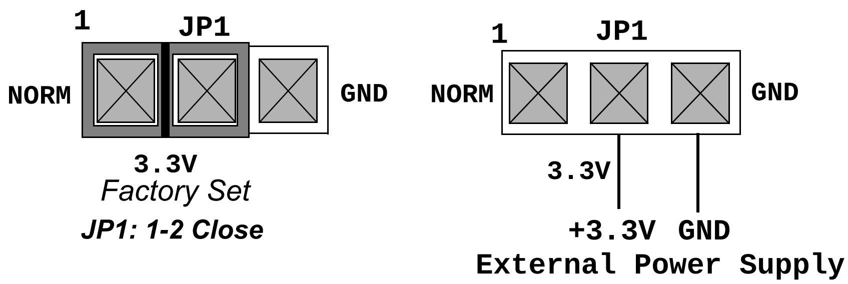


Figure 1-1 JP1 - CODEC Power Selection

1.2.2 JP2,JP3 - EE0,EE1 for Slave

JP2 and JP3 may be used for debugging purposes - to measure/set MSC8102 signal logic levels.l

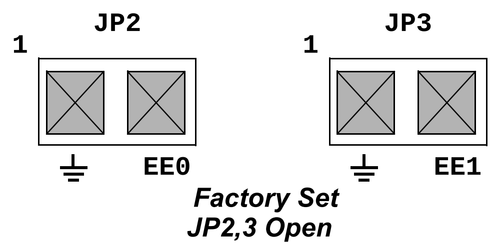


Figure 1-2 JP2,JP3 - EE0s,EE1s control

1.2.3 JP4 - Slave ClockOut Test Point

Using a scope, JP4 may be utilized for measuring a MSC8102 System Bus Clock.

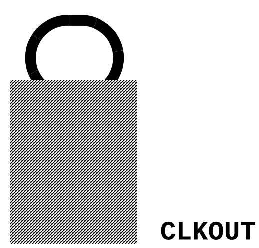


Figure 1-3 JP4 - MSC8102 ClockOut TP13

1.2.4 JP5 - External Clock Enable for MSC8102 TDM port

JP5 is used for MSC8102 TDM port test purposes. In the instance that jumper JP5 is closed, the TDM lines connect to the TSI & E1/T1 Framer devices and from there to expansion connector J5. If jumper JP5 is open then all TDM signals become available on J5 and, as a consequence, are isolated from other ADS sections..

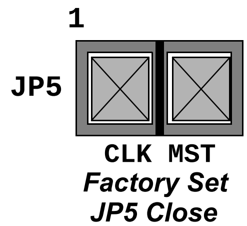


Figure 1-4 JP5 - TDM External Clock Enable

1.2.5 JP6 - CT-Bus Master Reset Enable

If the JP6 is closed then the MSC8102 applies Master Reset for the CT-bus (H.110)..

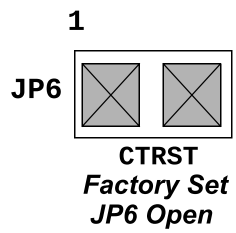


Figure 1-5 JP6 - CT-Bus Master Reset Enable

1.2.6 JP7 - ADS PON Reset Enable

If JP7 is closed then the ADS exists in a Power-On-Reset state that is used solely for debugging purposes..

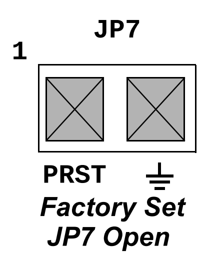


Figure 1-6 JP7 - ADS PON Reset Enable

Section 2 General Information

2.1 Introduction

This user guide describes the engineering specifications of the MSC8102ADS board. The board is based on the MSC8102 - a highly integrated system-on-a-chip device containing four StarCore SC140 DSP Cores. The System Interface Unit (SIU) for the MSC8102 is similar to that of the MSC8101.

The board is intended to serve as a platform for software (s/w) and hardware (h/w) development in the MSC8102 processor environment. On-board resources and the associated debugger enable developers to perform a variety of tasks: download and run code; set breakpoints; display memory and registers; and, connect proprietary h/w via the expansion connectors. The MSC8102 processor enables the incorporation of these features into selected systems.

The ADS may be used as a demonstration tool. For example, application s/w may be burned[A] into the ADS' flash memory and run in exhibitions. ADS boards are produced with two configurations - the "Complete" configuration provides host processor features while the "Single" configuration is used solely for evaluating the MSC8102.

2.2 List of Abbreviations

- **ADS** - MSC8102ADS, the document subject
- **BCSR** - Board Control & Status Register
- **CPM** - Communication Processor Module
- **CW** - Metrowerks CodeWarrior IDE for StarCore
- **DIP** - Dual-In-Line Package
- **DMA** - Direct Memory Access
- **DSI** - Direct Slave Interface
- **GPCM** - Memory Controller General Purpose Chip-select Machine
- **GPL** - General Purpose Line (associated with a UPM)
- **HCW** - Hardware Configuration Word
- **SDRAM Machine** - Memory Controller Synchronous Dynamic RAM Machine
- **UPM** - Memory Controller User Programmable Machine
- **ZD** - Clock Zero Delay Buffer with internal PLL for skew elimination

2.3 Related Documentation

[1] *MSC8102 - MSC8102 Specification*

[2] *MSC8101 Data Sheet*

[3] *SWITI Switching Device PEF24471 HTSI-XL. Wired Communication. Data Sheet.*

A. Either on-board or off-board.

2.4 Board Specifications

Specifications for the MSC8102ADS are provided below in *Table 2-1*.

Table 2-1 MSC8102ADS Specifications

CHARACTERISTICS	SPECIFICATIONS
Power requirements	9-18V external DC power supply. For 12V max current 1.2A
MSC8101/MSC8102 multicore (4xSC140 core) DSP	Internal clock runs up to 300MHz @ 1.6V
MSC8101 (Host-side) 60x Bus (DSI) MSC8102 (Slave-side) System Bus	System and 60x Buses both running up to 100 MHz Clock Frequency.
MSC8101: PowerPC (60x) bus: Local Bus: Addressing: Data Bus Width: MSC8102 DSI bus (non-buffered). SDRAM 100MHz soldered (non-buffered) Flash memory (buffered) BCSR (buffered) AMT Framer (buffered) MSC8102 System Bus: Addressing: SDRAM 100MHz soldered (non-buffered). 64-bit configuration 32-bit configuration Flash memory (buffered)	 4GB (32 address lines) @ 64bit Data External Decoding: 16MB (24 address lines) Internal Decoding: 4GB (32 address lines) 64-bit 2MB organized as 32-bit (default conf.) or 64-bit. 16MB,organized on two devices 4Bank x 4Meg x 32-bit. 4MB, 16-bits wide. BCSR contains eight byte-size registers. 1KB, 8-bits wide. 64/32 -bit - dependant upon the configuration mode 4GB (32 address lines) 16MB on two devices 4Bank x 4Meg x 32-bit 8MB on a single device 4Bank x 4Meg x 32-bit 4MB organized 4Meg x 8-bit
Operating temperature	0^{o}C - 30^{o}C (room temperature)
Storage temperature	-25^{o}C to 85^{o}C
Relative humidity	5% to 90% (non-condensing)
Dimensions require 6U CompactPCI® form factor with: Length Width Thickness	 233.35 mm 160.0 mm 1.8 mm

2.5 ADS Features

- **The ADS is based on the 64-bit MSC8102. Both the System and Direct Slave Interface (DSI) buses run up to 100MHz.**

- **Note that the Host controller MSC8101 and 60-x bus interface with Slave MSC8102 and its DSI bus.**

- **ADS Configurations:**
    - o MSC8102ADS: “Complete” configuration includes a host controller.
    - o MSC8102ADSs: “Single” configuration is without both host controller and peripherals. Only the MSC8102 is populated.
- **The MSC8102 Interface:**
    - o DSI bus is a slave of the MSC8101 with its 60-x bus.
    - o DSI may be configured to 32-bit when the System bus is sized at 64-bit (default mode) or visa versa (DSI 64-bit/System bus 32-bit).
    - o The Memory Controller Synchronous Dynamic RAM (SDRAM) Machine controls either 8 or 16MB of SDRAM memory size on the System bus. The size of memory is dependant upon the System’s bus configuration.
    - o Features a 4MB @ 8-bit size Flash for configuration/boot/program storage.
    - o Four MSC8102 TDM ports are connected to the Infineon TSI PEF24471 device. The device allows the interconnecting of T1/E1 time-slots between the Infineon FALC PEB2256 and the Dual CODEC MT92303. An interface with the H.110 TDM bus on the J4 Compact PCI connector is also available.
    - o RS232 Transceiver MAX3241 supports the UART port operation of the MSC8102.
- **The MSC8101 Interface:**
    - o Acts as a host for the MSC8102.
    - o SDRAM machine controls 16MB SDRAM on 60-x bus.
    - o Features a 4MB @16-bit size Flash for configuration/boot/program storage.
    - o Communication Processor Module (CPM) ports are connected to the following: ATM Framer PM5384 with Optical I/F (FCC1); 10/100 Base-T Phy L80225 of LSI Logic (FCC2); RS232 Transceiver MAX3241(SCC1).
    - o An 8-bit Board Control & Status Register (BCSR) is required for MSC8102ADSc configuration.
- **Board Capabilities:**
    - o Programmable Hard Reset Configuration for MSC8102 is executed from the Flash memory or the DSI bus. This configuration type may also be forced from the BCSR.
    - o Boot for the MSC8102 is available from the Host controller via the DSI bus and from the System bus (Flash). Boot may also be performed from the UART or TDM ports.
    - o To facilitate the measuring of MSC8102 signals, high density (MICTOR) Logic Analyzer connectors are used.
    - o When used as expansion connectors, CompactPCI® connectors J1,J2 and J5 carry MSC8102 signals to off-board tools thus enabling chip verification and evaluation.
    - o Debugging is performed via an external Command Converter that is connected ei-

ther to both of the OnCE 14-pin headers or, alternatively, to one or the other of them. There is one OnCE 14-pin header for each processor.

- The OnCE debug chain allows, via backplane, the connection of additional ADS boards.
- After reset the Debug Enable/Disable and Debug Request options may be selected. The processor's EE pins enable and support the noted options.
- Board Identification and board status may be read via the BCSR.
- An SMB form RF-connector enables the connection of an external pulse generator to the clock input of the MSC8102.
- Variant board configurations are made available via the Dual-In-Line Package (DIP) Switch setting.
- The board features push buttons for both the Host and Slave: Power-On Reset; Soft Reset; Hard Reset; and, ABORT.
- The board is powered by a single 9 - 18V external DC Supply with on-board reverse polarity protection.
- Voltage is provided to the board's DC-DC Converter. The Converter has the following parameters: 3.3V @ 4A 10%.
- The DC-DC Converter powers two voltage regulators: 1.3 - 1.7V adjustable linear voltage regulator for the MSC8102; and, the 1.6V linear voltage regulator for the MSC8101.
- The Software Option Switch provides 8 s/w options via the BCSR.
- The LED's indicate the following: power supply; peripheral enables; EE1-pin status; and, s/w signals.

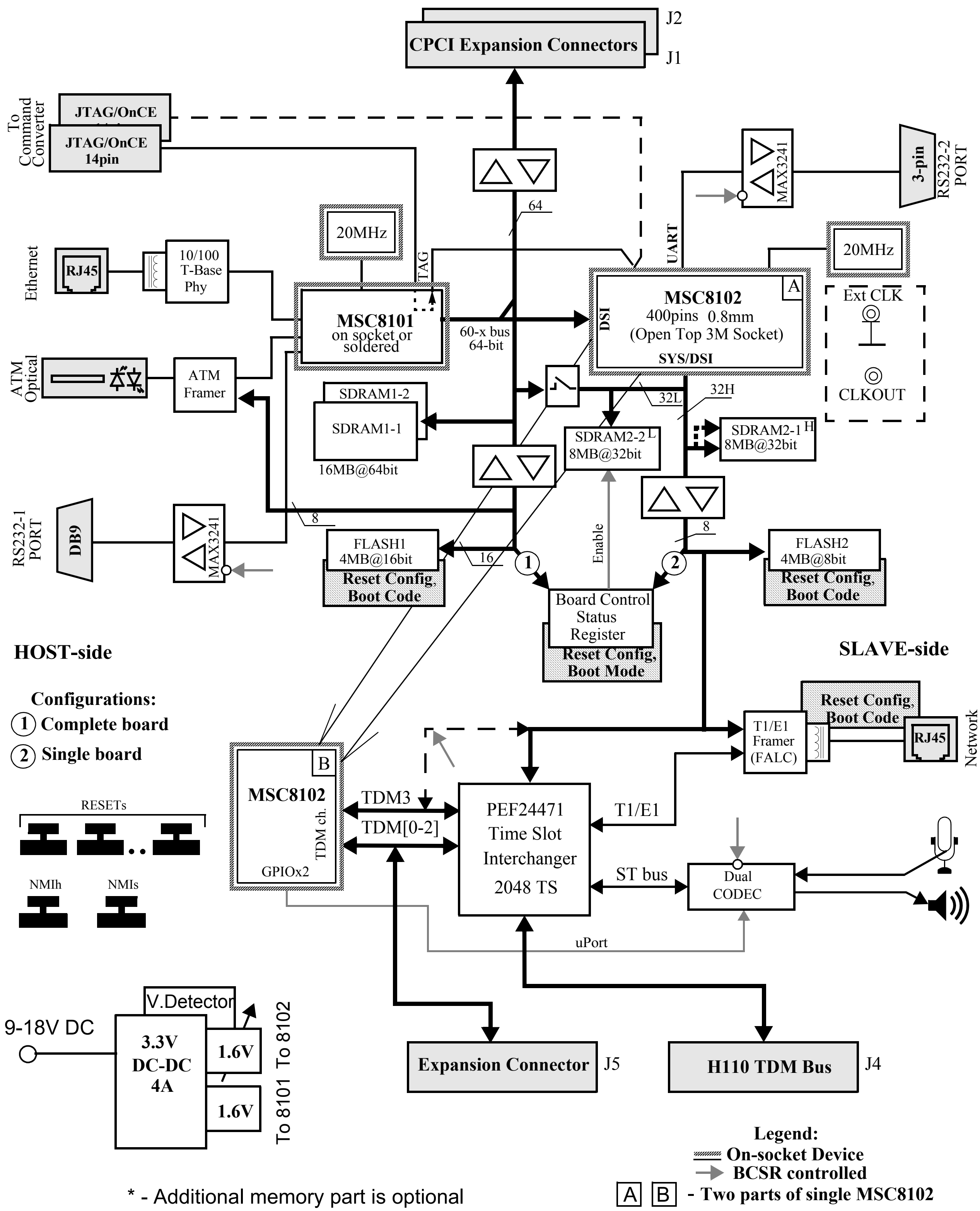


Figure 2-1 System Block Diagram

Section 3 Configuration and Installation

3.1 Hardware Preparation

This chapter contains installation instructions for the MSC8102ADS board.

CAUTION:

Be sure to switch off or disconnect power when reconfiguring an installed ADS board. Reconfiguring jumpers with the power on can damage system circuits.

When you unpack the MSC8102ADS board from its shipping carton, refer to the packing list to verify that all items are present and in good condition.

NOTE: *If the ADS board arrives damaged, save all packing material and contact the carrier's agent.*

Parts locations on the ADS board are shows in the Figure 3-1 MSC8102ADS Top-side Part Location Diagram.

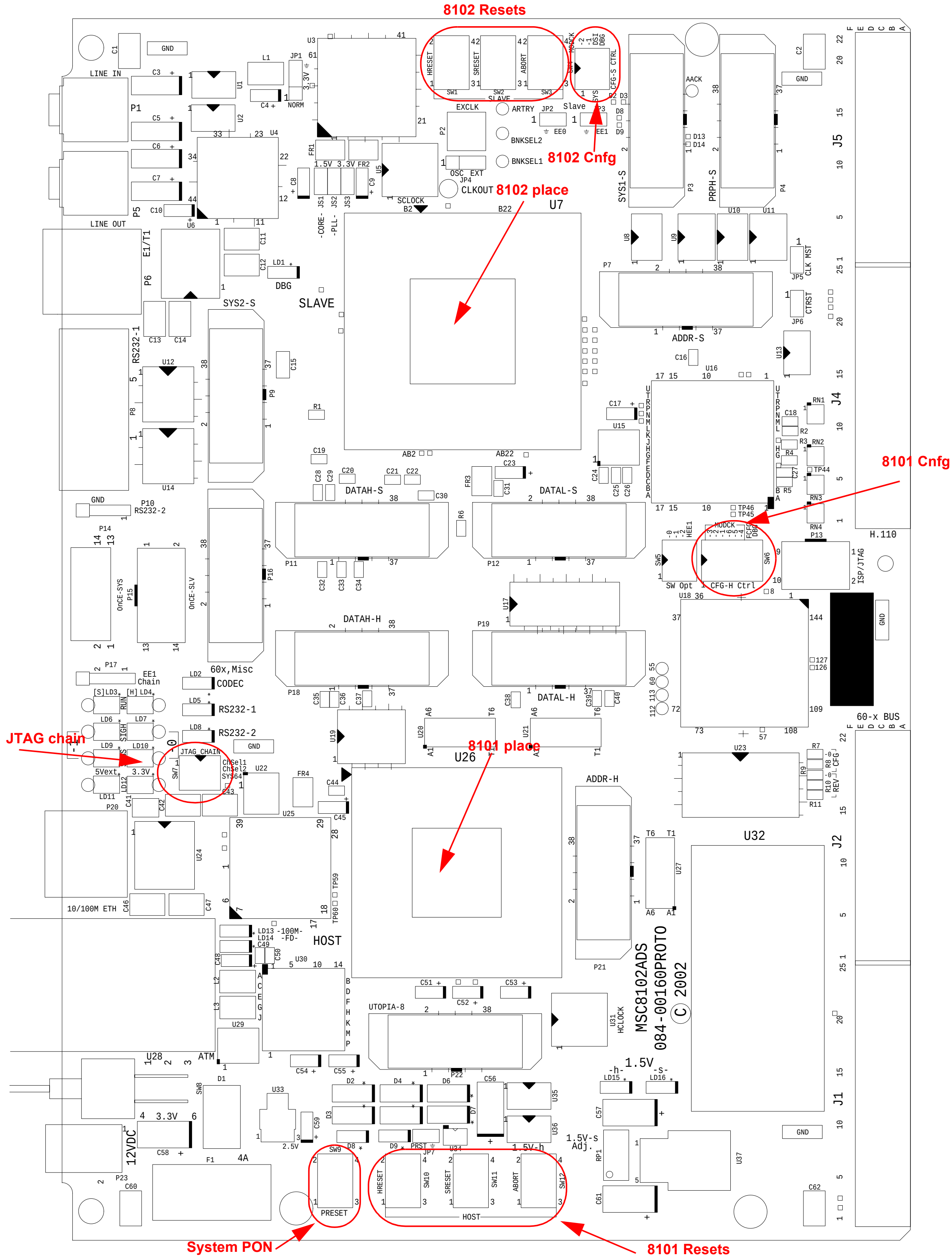
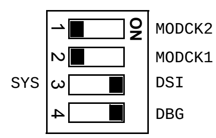
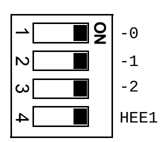


Figure 3-1 MSC8102ADS Top-side Part Location Diagram

3.1.1 Switches

ADS Dual-In-Line Package (DIP) Switches and push buttons are listed and described in Table 3-1 The ADS Switches and Table 3-2 The ADS Push Buttons, respectively. The switches and jumpers featured in this chapter are shown with their factory-default positions. ADS board LED's are also detailed.

Table 3-1 The ADS Switches

Designator & Purpose	Type	Description
SW4 Slave Configuration Control (MSC8102)	 CFG-S Ctrl	**SW4.1-SW4.2** set the MODCK1,2 of MSC8102 Slave to the PLL mode. When "ON", the value is zero. When there is a clock-in frequency of 41.6MHz, the clock mode is set to 11. **SW4.3** (SYS <-> DSI) selects the power-up configuration source. MSC8101 Host is the configuration source when the DSI position is chosen. If SYS is selected then the MSC8102 Slave Flash is the configuration source. **SW4.4** While in DBG position, EE0 input is high at the time of Core reset. This allows the Cores to enter Debug mode immediately after negation of HRESETs. When not in the DBG position then, after reset, the Cores run freely. The Debug mode may be activated by toggling SW4/4. Factory settings: - MODCK1,2 are OFF - Config source from DSI - Debug mode after Slave's Hard Reset
SW5 Software Option reading by MSC8101	 SW Opt	**SW5.1-SW5.3** set Software Option Bits 0-2 for SW flow control. When "ON", the value is zero. **SW5.4** is used for Host EE1 pin control after Power-On-Reset. When "ON", the value is zero. Reset Factory settings: - All bits set to ON

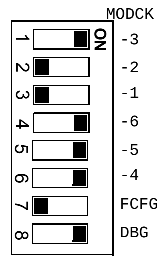
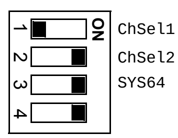
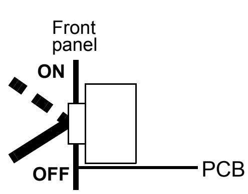
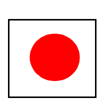
SW6 Host Configuration Control (MSC8101)	 CFG-H Ctrl	**SW6.1-SW6.6** set the MODCK1-6 of MSC8101 Host to the PLL mode. When “ON”, the value is zero. When there is a clock-in frequency of 55MHz, the clock mode is set to 57. **SW6.7** sets HCW1 source. When “ON” the source is Host Flash. If “OFF” then the source is a BCSR programmed value. **SW6.8** While in DBG position, EE0 input is high at the time of Core reset. This allows the Core to enter Debug mode immediately after negation of HRESETh. When not in the DBG position then, after reset, the Core runs freely. The Debug mode may be activated by toggling SW6/8. Reset Factory settings: -Clock Mode is 57 -HCW1 originates from BCSR -Debug Enable after Host Hard Reset
SW7 JTAG Chain Setting	 JTAG_CHAIN	**SW7.1-SW7.2** set the JTAG Chain configuration Bits 1-2. ChSel: 1 2 “ON” “ON” - Separate JTAG Access “OFF” “ON” - Short JTAG Chain “OFF” “OFF” - Long JTAG Chain **SW7.3** sets the Slave’s System Bus width. When “ON” the System Data Bus of the MSC8102 is 64-bit and the DSI bus is 32-bit. If “OFF” then the System Bus is 32-bit and the DSI bus is 64-bit. **SW7.4** Reserved. Reset Factory settings: -Short JTAG Chain -MSC8102 System Bus 64-bit The “JTAG Command Converter” plugs into the front of connector P14.
SW8 Power Switch	 	**SW8** When in the “ON” position power comes from an external 12V Power Supply via a P23 connector. When “OFF” the external power supply via P23 is disconnected. Consequently, when located in the CPCI backplane, the ADS is then powered by an internal power supply via cPCI connectors.

Table 3-2 The ADS Push Buttons

SW1 Slave Hard Reset	 HRESET	Pressing button SW1 results in Hard Reset for the MSC8102 (HRESETh is asserted).

SW2 Slave Soft Reset	SRESET	Pressing button SW2 results in Soft Reset for MSC8102. Despite the reset, clock and chip-select data as well as SDRAM contents are retained. Soft Reset causes the Slave's cores to run free despite the position of SW4/4.
SW3 Slave NMI (IRQ0)	ABORT	Pressing and releasing button SW3 results in a non-maskable interrupt for MSC8102.
SW9 Power-On-Reset (PORESET)	PRESET	Pressing button SW9 results in main Power-On-Reset for both processors, MSC8101 and MSC8102.
SW10 Host Hard Reset	HRESET	Pressing button SW10 results in Hard Reset for MSC8101. Host Hard Reset produces Power-On-Reset for MSC8102.
SW11 Host Soft Reset	SRESET	Pressing button SW11 results in Soft Reset for MSC8101. Despite the reset, clock and chip-select data as well as SDRAM contents are retained. Soft Reset causes the Host's core to run free despite the position of SW6/8.
SW12 Host NMI (IRQ0)	ABORT	Pressing and releasing button SW12 results in an non-maskable interrupt for MSC8101.

3.1.2 Jumpers

MSC8102ADS jumpers will be noted in the following sub-sections:

3.1.2.1 JP1 - External Power for CODEC

JP1 selects the source for the CODEC Power Rail. When a jumper is located between pins **1 - 2 of JP1** (Factory Set) then the CODEC feeds from the 3.3V plane of the ADS.

When a jumper is removed the 3.3V @ 200 mA external low-noise power supply may be connected to JP1 pins 2-3 as illustrated below in. Figure 3-2 JP1 - CODEC Power Selection.

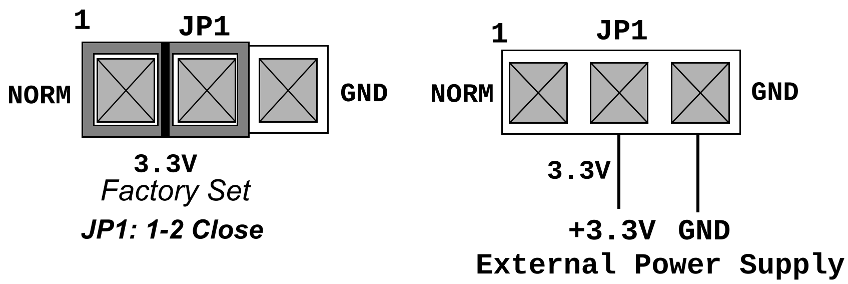


Figure 3-2 JP1 - CODEC Power Selection

3.1.2.2 JP2,JP3 - EE0,EE1 for Slave

JP2 and JP3 may be used for debugging purposes - to measure/set MSC8102 signal logic levels.l

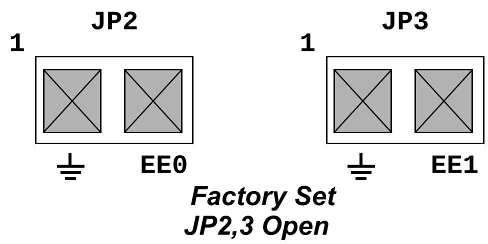


Figure 3-3 JP2,JP3 - EE0s,EE1s control

3.1.2.3 JP4 - Slave Clock Input Source

JP4 is used to select clock input source for MSC8102 either mounted on socket clock oscillator or external pulse generator via P2 SMB connector.

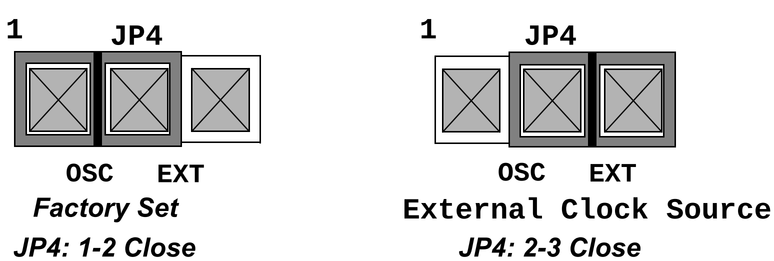


Figure 3-4 JP4 - MSC8102 Clock Source Select

3.1.2.4 JP5 - External Clock Enable for MSC8102 TDM port

JP5 is used for MSC8102 TDM port test purposes. In the instance that jumper JP5 is closed, the TDM lines connect to the TSI & E1/T1 Framer devices and from there to expansion connector J5. If jumper JP5 is open then all TDM signals become available on J5 and, as a consequence,

are isolated from other ADS sections..

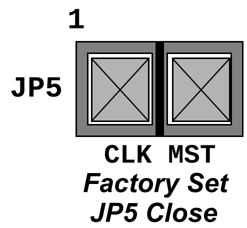


Figure 3-5 JP5 - TDM External Clock Enable

3.1.2.5 JP6 - CT-Bus Master Reset Enable

If the JP6 is closed then the MSC8102 applies Master Reset for the CT-bus (H.110)..

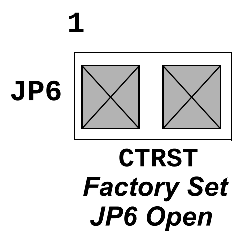


Figure 3-6 JP6 - CT-Bus Master Reset Enable

3.1.2.6 JP7 - ADS PON Reset Enable

If JP7 is closed then the ADS exists in a Power-On-Reset state that is used solely for debugging purposes..

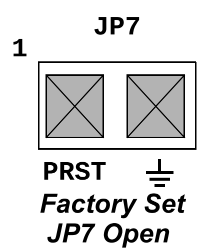


Figure 3-7 JP7 - ADS PON Reset Enable

3.1.2.7 JS1-3 - Current Consumption Measurement

JS1 to 3 reside, respectively, on the following: the core; the PLL; and, the I/O-pin’s main flow. To measure current consumption the relevant JS must be removed using a soldering tool. Follow-

ing this a current meter (or a shunt) is connected using the shortest and thickest wires available.

Warning

The delicate task of removing JS1 to 3 should only be performed by a skilled technician. The MSC8102ADS may suffer permanent damage if an unskilled hand makes more than 3 attempts at the change.

3.1.2.8 JG1-5 GND Bridges

The MSC8102ADS has 5 bridges designated as GND. They are meant to assist in general measurements and act as logic-analyzer connections.

Warning

Use only INSULATED GND clips when connecting to a GND bridge as, otherwise, permanent damage may occur to the MSC8102ADS. Non-insulated clips coming into contact with surrounding "HOT" points may create short-circuits.

3.1.2.9 TP13 - Slave Clock Output

Using a scope, TP13 may be utilized for measuring a MSC8102 System Bus Clock.

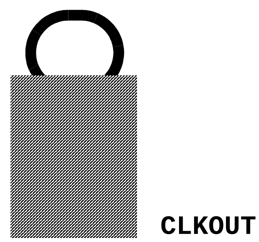


Figure 3-8 TP13 - MSC8102 ClockOut

3.1.3 LEDs

The MSC8102 has the following LEDs:

3.1.3.1 LD1 - Slave in Debug Mode

The debug acknowledge function of the EE1 pin found on the MSC8102 is indicated by a green LED, LD1. When lit, the MSC8102 is either in Debug Mode or there is a high level of EE0 input (debug request).

3.1.3.2 LD2 - CODEC

A yellow LED, LD2, indicates that the CODEC device is ready for programming. The CODEC is controlled by bit BCSR0.3.

3.1.3.3 LD3 - Slave is running

A **green** LED, LD3, indicates that the MSC8102 is accessing the external System Bus by reading/writing to the bus devices.

3.1.3.4 LD4 - Host is running

A **green** LED, LD4, indicates that the MSC8101 is accessing the external 60-x bus by reading/writing to the bus devices.

3.1.3.5 LD5 - RS232-1 Enable

A yellow LED, LD5, indicates whether the Host's RS232 Transceiver has been enabled (lit) or disabled. The RS232 is controlled by bit BCSR1.6.

3.1.3.6 LD6, LD7 - Host Signaling LEDs

LED's, LD6 (**red**) and LD7 (**green**), are program controlled. They are used for extra visibility on the Host- running utility. They are lit up by setting bits BCSR0.6-7.

3.1.3.7 LD8 - RS232-2 Enable

An activated yellow LED, LD6, indicates that the Slave RS232 Transceiver is enabled. If disabled, the MSC8102 UART pins may be used for off-board applications via the J5 expansion connector. The RS232 is controlled by bit BCSR1.7.

3.1.3.8 LD9, LD10 - Slave Signaling LEDs

LED's LD9 (**red**) and LD10 (**green**) are MSC8101 program controlled. They are used for extra visibility on the Slave MSC8102 running utility. The LED's are lit by setting bits BCSR0.4-5.

3.1.3.9 LD11 - External Power Indicator

When the ADS is inserted into the cPCI rack, a **green** LED, LD11, indicates a 5V presence from the backplane power supply. The ADS is powered from the backplane power supply whenever the SW8 Power Switch has been turned to the “OFF” (down) position.

3.1.3.10 LD12 - 3.3V Power Indicator

A 12V power supply is plugged into the P23 Power Connector on the board's front side. The ADS is powered by the 12V power supply when the SW8 Power Switch is turned to the “ON” (up) position. The **green** LED, LD12, indicates a 3.3V power level (from the available 12V power supply).

3.1.3.11 LD13, LD14 - Ethernet Indications

The **green** LED, LD13, indicates a 100MBps operation mode. The **green** LED LD14 indicates a full duplex mode. Two additional Ethernet LEDs are mounted inside connector P20 RJ45 - a **green** LED indicative of an existing “LINK” as well as a **red** LED that serves as a ”COLLISION” indicator.

3.1.3.12 LD15, LD16 - 1.5V Power Indicator

Green LED's, LD15 and LD16 indicate, respectively, the presence of a 1.5V power supply for

the core and PLL of the Host and Slave processors.

3.2 Installation Options

Configure the ADS board according to its environment:

- Host Controlled Operation through OnCE port
- Stand-alone mode

3.2.1 Debug Connection Schemes

In the Debug Connection Scheme configuration the MSC8102ADS is controlled by a host computer via the OnCE Port, a subset of a JTAG port. This configuration allows for extensive debugging using an on-host debugger. The Host is connected to the ADS via a Command Converter provided by a third party such as Macraigor Systems. A PCI host debug interface is preferred due to the faster throughput offered by a parallel port interface. Three possible connections are shown in the figures below: Figure 3-9 Host System Debug Scheme A (spitted), Figure 3-10 Host System Debug Scheme B (daisy-chained) and Figure 3-11 Host System Debug Scheme C (daisy-chained).

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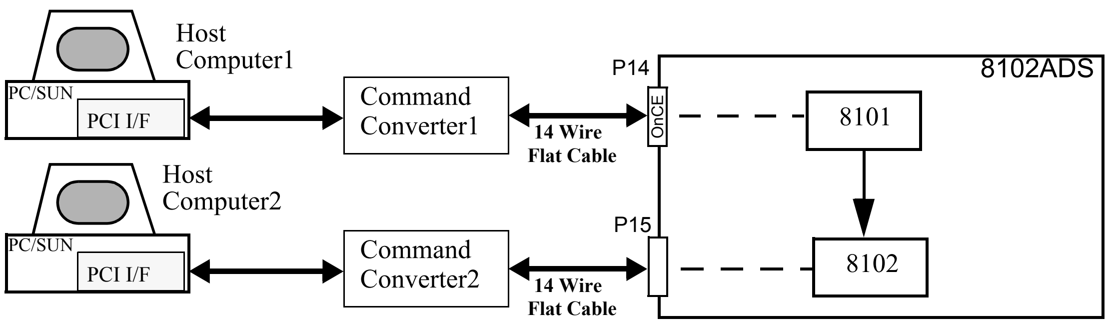


Figure 3-9 Host System Debug Scheme A (spitted)

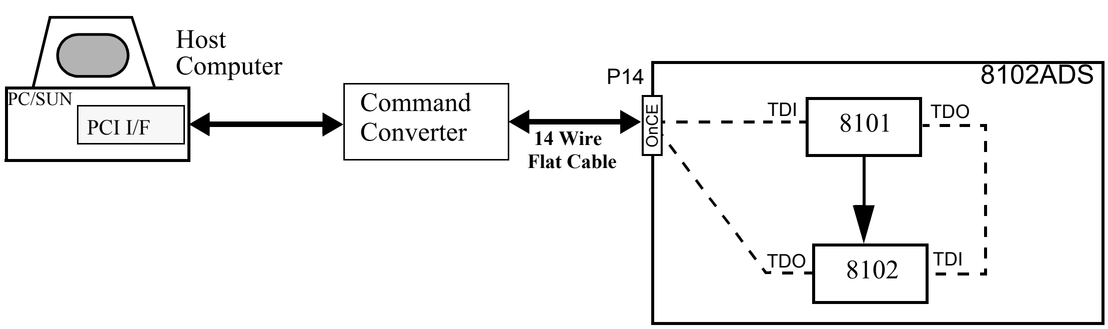


Figure 3-10 Host System Debug Scheme B (daisy-chained)

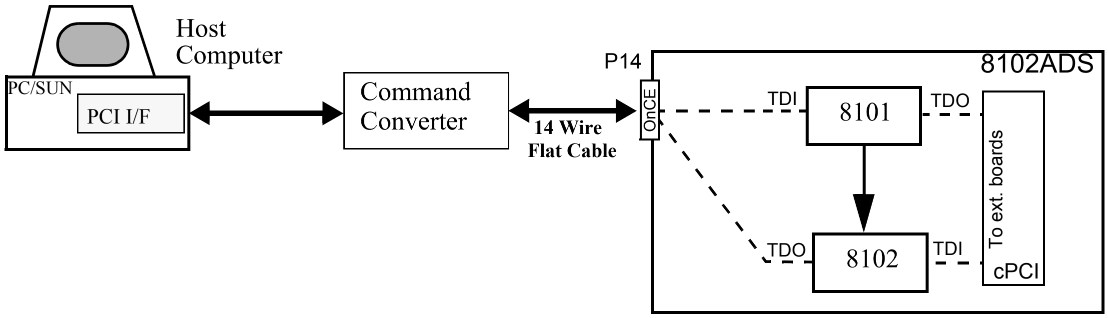


Figure 3-11 Host System Debug Scheme C (daisy-chained)

Figure 3-12 JTAG-Chain on Backplane, below, illustrates a debug configuration. This debug configuration enables evaluation of the DSP farm concept. The concept sees one ADS Host processor (MSC8101) with Slave (MSC8102) and three ADSs Slaves (MSC8102) placed on a total of four boards. These boards are then mounted onto a standard CompactPCI® backplane that provides required interconnections.

The EE-pins, EE0 and EE1, of the MSC8102 are placed on the ADS front panel. When these pins are connected, as shown below in Figure 3-12, all the slaves simultaneously enter Debug mode. The connection is made by a specific (made-to-order) pin-to-pin cable..

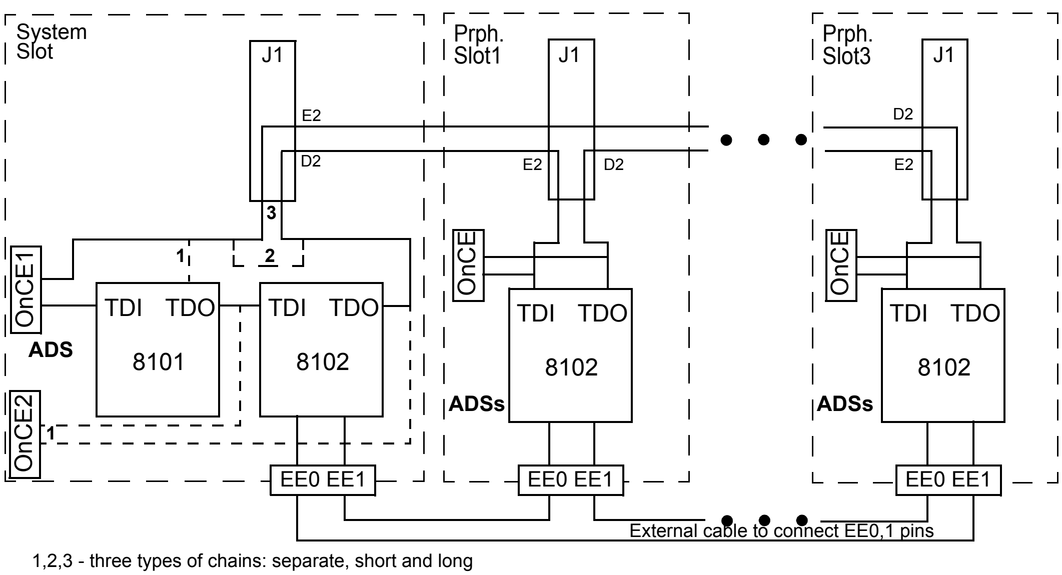


Figure 3-12 JTAG-Chain on Backplane

3.2.2 Standalone Operation

In the standalone mode, the Host does not control the ADS via the OnCE port. Rather, the ADS may be connected to the Host via alternate ports - RS232 (either from Host or from Slave), Fast Ethernet, ATM155, etc. Operating in standalone mode necessitates burning the application program into the board's Flash memory (either the Host's or the Slave's). In the instance of a single board configuration, the DSI bus is used to connect with the Host.

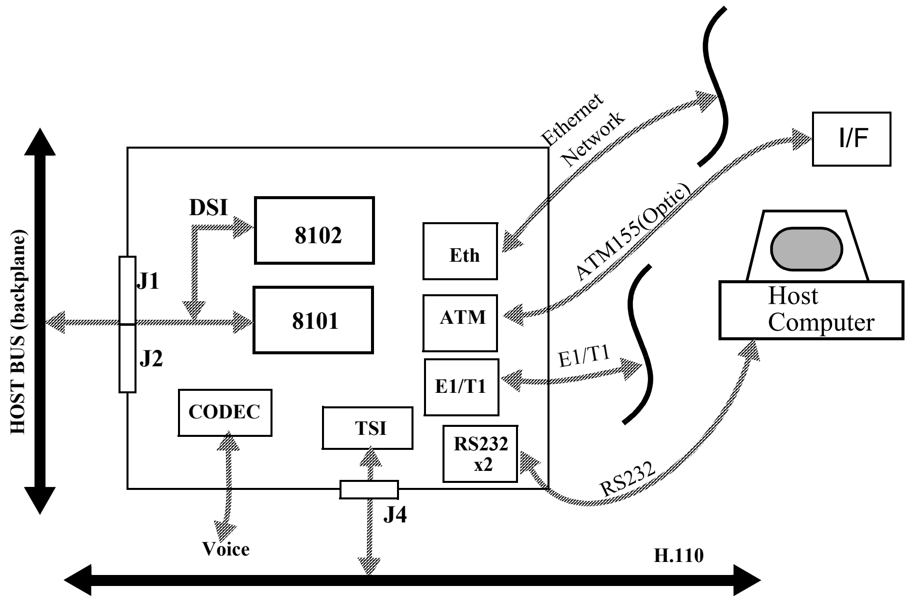


Figure 3-13 Standalone Configuration (ADS board)

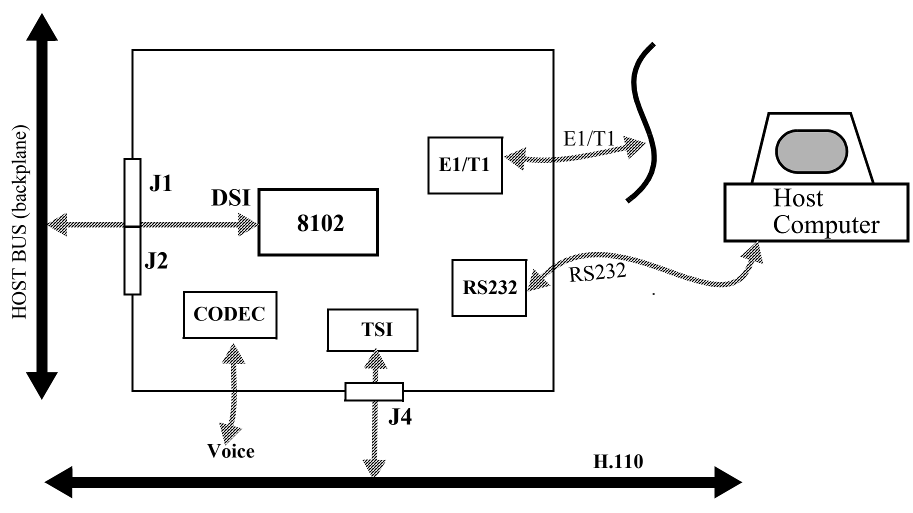


Figure 3-14 Standalone Configuration (ADSs board)

The 60-x bus of an MSC8101 or an MPC8260 may be used as the host bus for the Single board (ADSs) standalone configuration. The ADS can provide a direct connection through the J1/J2 con-

nectors to the DSI bus of the MSC8102 on the ADSs board. To this purpose it is possible to use a general 6U CompactPCI® rack with a single system board such as the ADS and several ADSs boards.

3.3 Connecting the ADS Board

The ADS board should be resides at working desk in a convenient place for connecting it to the Host computer and external power supply.

Connect the ADS as follows:

1) Connect the External Command Converter to the front “OnCE” (P14) connector for B and C debug scheme (Figure 3-10 and Figure 3-11) and to P14 and/or to header P15 for A debug sheme (Figure 3-9).
2) Connect an external power supply to P23 power jack on the ADS.
3) Plug in the external power supply to the ~110-240VAC wall outlet.
4) Switch on SW8 Power on the ADS board, upper LED “PWR” (LD12) will lights up.

3.4 Power Supply

The MSC8102ADS requires +12VDC @ 1.8A max, power supply. The power may be provided via cPCI expansion connectors when the ADS is placed into backplane.

To apply power source insert enclosed power supply plug into the P23 Power Jack on the board as shows in the Figure 3-15 Ext Power Supply Connection.

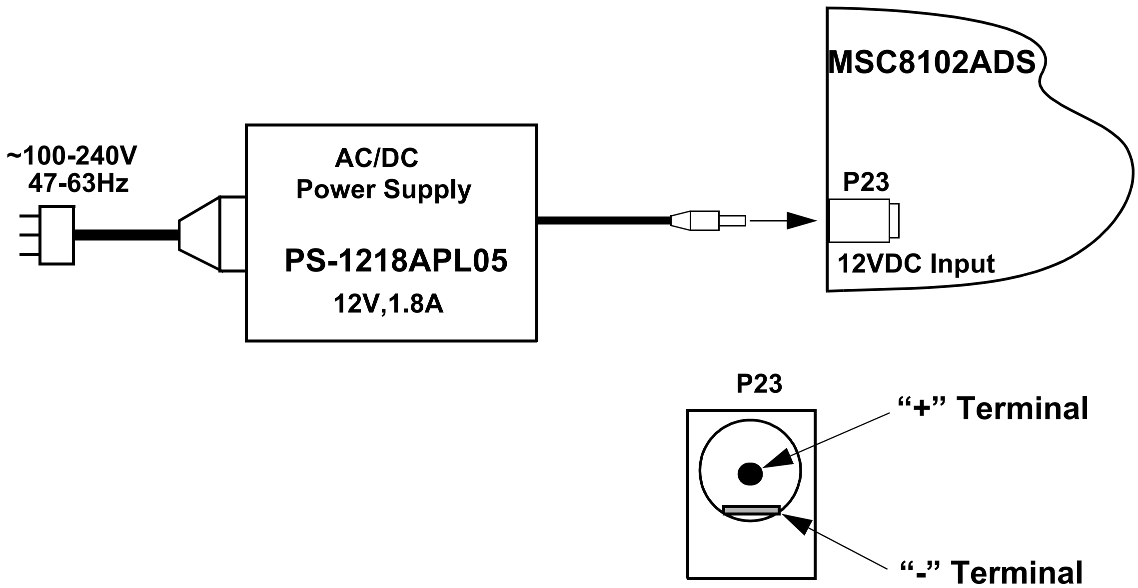


Figure 3-15 Ext Power Supply Connection

NOTE: *It is allow to connect users hardware applications to the ADS board using cPCI Expantion Connectors J1,J2,J4,J5 connectors. Therefore, take additional power requirements into consideration when using an enclosed power supply.*

In order the ADS is inside cPCI rack power may be applied from build-in power supply when ADS switch SW8 is turned to the "OFF" (down) position as shows in the Figure 3-16 Power on Backplane. On Front Panel lower "PWR" LED indicates that power from backplane is "good".

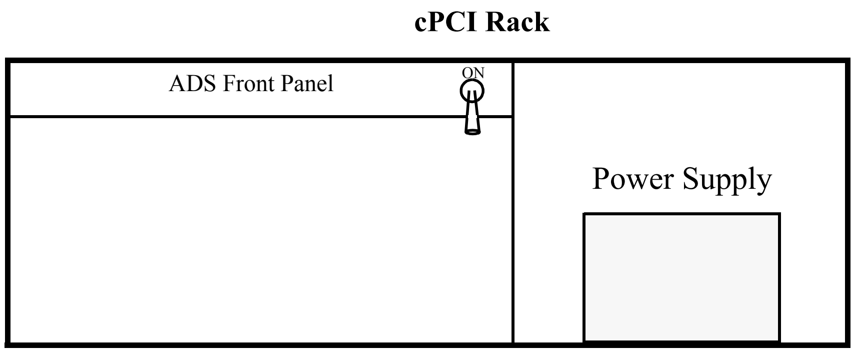


Figure 3-16 Power on Backplane

Section 4 Functional Description

4.1 General

This chapter describes, in detail, the ADS block diagram. There are two ADS configurations based on MSC8102. The full ADS configuration, MSC8102ADS, consists of two sides: the Host, based on MSC8101 as host controller; and, the Slave, based on the MSC8102. The second configuration is a single board based on only one processor, the MSC8102.

The MSC8102 is interfaced to the Host via a DSI bus that is connected asynchronously to the 60-x bus of the MSC8101. The DSI bus is accessible to external tools via the J1/J2 expansion connectors. An additional expansion connector, J5, provides connectivity to four TDM ports - the UART, the Timers, the Interrupts and the GPIO of the MSC8102. The J4 expansion connector interfaces with the standard H.110 bus (ECTF H.110 Specification). The 32-bit DSI data bus (default) may be reconfiged during Power-on-Reset to 64-bit. At the same time, the 64-bit System Data Bus becomes 32-bit.

The address bus switch for the SDRAM is located on the MSC8102's System Bus. This switch provides correct connections for both the 64-bit and 32-bit data bus configurations.

4.2 Reset & Reset - Configuration

The Reset signals for the MSC8102ADS are produced by either the MSC8101 or MSC8102 controllers. Reset circuitry details are shown below in *Figure 4-1 "ADS Reset Diagram"*:

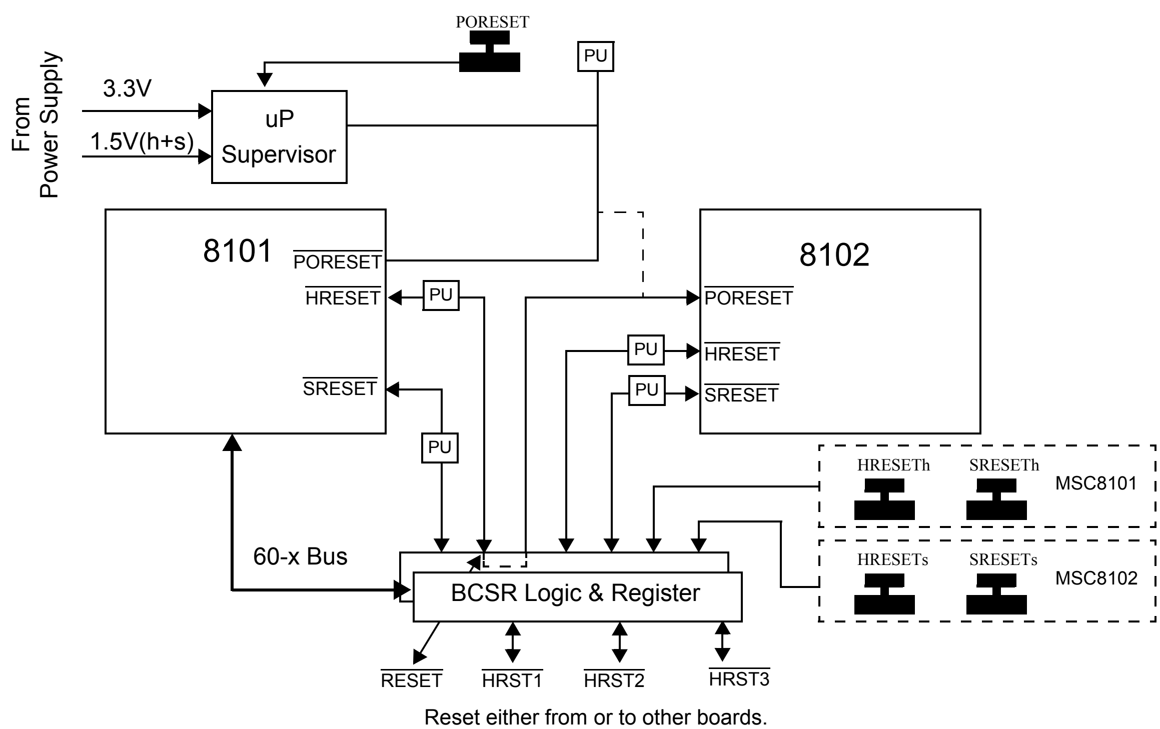


Figure 4-1 ADS Reset Diagram

4.2.1 Power-On-Reset

The MSC8102ADS main Power-On-Reset button initializes both the Host processor and the Slave state after power up. The initialization involves dedicated logic that uses MAX6827 - a dual uP supervisor looking after one 3.3V and two 1.5V power rails that keep the processors supplying nominal power. The dual uP supervisor has open-drain output circuitry that allows for off-board RESET sources such as the *one-shot*. The PORESET impulse for the MSC8102 is driven by BCSR logic and will either be asserted during MSC8101 HRESET or activated by programming the BCSR register. See *Table 4-11 "BCSR2 Register Description" on page 66* for details.

Main Power-On-Reset is asserted to the MSC8101 for a period of 350msec. This provides ample time to cover voltage regulator stabilization. Power-On-Reset may be generated either manually or by a dedicated push-button connected to the manual reset input of the supervisor device.

4.2.2 Host Power-On-Reset Configuration

Upon completion of the Power-On-Reset sequence the MSC8101 samples MODCK(1:3) together with three additional clock configuration bits. In addition, various MSC8101 system (dsp core, cpm, 60x bus) clock modes are set. The MODCK(1:3) combination options are controlled by DIP Switches SW6/1-6 and are buffered via BCSR logic.

Following Power-On-Reset is the Hard Reset sequence within which a multitude of other options are configured. MODCK bits are sampled during Hard Reset configuration as well as each time a Hard Reset sequence is entered, however, they are influential only once - after Power-On-Reset. If a Hard Reset sequence is later entered then the bits, though sampled, have no impact.

4.2.3 Slave Power-On-Reset Configuration

Upon concluding the Power-On-Reset sequence the MSC8102 samples the MODCK(1:2) together with three additional clock configuration bits. It should be noted that various MSC8102 system (dsp cores, 60x bus) clock modes are also set. MODCK(1:2) combination options are controlled by DIP Switches SW4/1-2 and are buffered via BCSR logic. At the time of Power-On-Reset some pins will be sampled. The complete setting can be seen in *Table 4-3*. The Reset signals for the MSC8102ADS are produced by either the MSC8101 or MSC8102 controllers. Reset circuitry details are shown above in *Figure 4-1 "ADS Reset Diagram"*. MSC8102 may also be configured via Host MSC8101 by writing the Power-on-Reset Configuration to BCSR and setting bit BCSR1.0 (RECONF) to 0. This will invoke secondary Power-On-Reset for the MSC8102.

Following Power-On-Reset is the Hard Reset sequence within which a multitude of options are configured. MODCK bits are sampled during Hard Reset configuration as well as during the first Hard Reset sequence after a Power-On-Reset. However, during subsequent Hard Reset sequences the bits are sampled but deemed irrelevant.

4.2.4 Hard/Soft Reset Capabilities

Host processor Hard Reset is available in the debug mode via JTAG/ONCE with a command from the host debugger system, Metrowerks CodeWarrior (CW). When Host HRESET is asserted then a MSC8102 PORESET impulse is generated automatically via BCSR logic. This occurs despite the reset systems for both processors, Host and Slave, being electrically isolated.

Dedicated push buttons facilitate manual Hard and Soft Reset for processors MSC8101 and MSC8102. These buttons enable run-time reset when the Command Converter is disconnected

from the MSC8102ADS.

The HRESET lines may be internally driven by the MSC8101/MSC8102 and as such must be driven to the MSC8101/MSC8102 with an open-drain gate.

When generating Hard Reset the registers of both processors are completely reset. For example, the Hard Reset configuration is re-sampled and all registers, including memory controllers but excepting PLL's, are reset. The reset results in a loss of dynamic memory content.

Off-board Slave DSP (max. of 4) Hard Reset signals are present in inputs from the BCSR register. Through programming, this allows for the separate monitoring and assertion of 8102 Slave resets.

4.2.5 Hard Reset Configuration

Hard Reset configuration is performed for both the Host (MSC8101) and Slave processors (MSC8102). In the case of the Single Board (ADSs), the Hardware Configuration Word (HCW) will be taken from the System bus to the MSC8102 device.

4.2.6 Host Hard Reset Configuration

Hard Reset, applied both externally and internally to the MSC8101, samples the HCW. The configuration word may originate from an internal default if the RSTCONF signal is negated during an HRESET assertion. It may also be taken from the 8101 Flash memory (MS 8-bits of the data bus) or from the BCSR board register[A] in the instance that the RSTCONF signal is asserted along with the HRESET.

If the 8101 Flash has been tampered with, then the default configuration word will be taken from either the Flash or the BCSR. A dedicated jumper determines whether the source of the default configuration word will be the FLASH or the BCSR.

During the Hard Reset sequence the configuration master reads, one byte at a time, the Flash (or BCSR) memory at addresses 0, 8, 0x18, 0x20 in order to assemble the 32-bit configuration word.

Table 4-1 Effect of Host (MSC8101) Pins on the Power-on-Reset Configuration

Name of signal	*Value*	*Mode*	*Implementation*
MODCK[1:3]	'101'	Set clock mode 40 (MSC8101 rev1)	DIP Switch SW6/1-3 setting. May be controlled by BCSR logic
RSTCONF	0	Boot Master from 60-x bus	Pulled-down permanently
EE0	0	Core running free after Hard Reset	DIP Switch SW6/8 setting (Debug Enable/Disable) via BCSR buffer
	1	Core enters Debug mode after Hard Reset	
EE1(HPE)	0	Host Port Disable - 60-x bus configured for 64-bit	Pulled-down permanently
EE[4:5](BTM[0:1])	'00'	Boot Source resides at 60-x bus	Pulled-down permanently

DIP Switch SW6/8 controls the EE0 pin in order to provide a post-reset manual debug capability

A. In general, reading from any device residing on CS0.

(Debug Request).

Table 4-2 "MSC8101 Hard Reset Configuration Word (HCW1)", below, describes the field values of the Hard Reset configuration word:

Table 4-2 MSC8101 Hard Reset Configuration Word (HCW1)

Field	*Data Bus Bits*	*Prog Value [Bin]*	*Implication*	*Offset In HCW source [Hex]*	*Value [Hex]*
EARB	0	'0'	Internal **Arbitration** Selected.	0	28
EXMC	1	'0'	Internal **Memory Controller.** $\overline{\text{CS0}}$ active at system boot.		
$\overline{\text{IRQ7INT}}$	2	'1'	**$\overline{\text{INT\_OUT}}$** function is active		
EBM	3	'0'	Single **chip bus mode** is assumed		
BPS	4:5	'10'	16-bit **Boot Port Size** for both Flash memory and BCSR		
SCDIS	6	'0'	**SC140** enabled		
ISPS	7	'0'	**Internal space port size** for external master access is 64-bit. Not of concern as the current board configuration does not support this feature.		
IRPC	8:9	'00'	**Interrupt pin configuration.** RES/BADDR(29)/$\overline{\text{IRQ2}}$,RES/BADDR(30)/$\overline{\text{IRQ3}}$, RES/BADDR(31)/$\overline{\text{IRQ5}}$ are selected as RES (not connect)	8	00
DPPC	10:11	'00'	**Data Parity Pin configuration** as $\overline{\text{IRQ}}$[1:7].		
NMIOUT	12	'0'	**NMI interrupt** is serviced by the core.		
ISB	13:15	'000'	IMMR initial value 0xF000_0000, i.e., initially **the internal space** resides at this address.		
Reserved	16	'0'	**Reserved.** Non-functional cleared bit.	10	32
BBD	17	'0'	**Bus busy** pins set as: $\overline{\text{ABB}}$/$\overline{\text{IRQ2}}$ pin is $\overline{\text{ABB}}$ DBB/IRQ3 pin is DBB		
MMR	18:19	'11'	**External Bus Request masked.**		
Reserved	20:21	'00'	**Reserved.** Must be cleared		
TCPC	22:23	'10'	**Transfer code** pins are configured following $\overline{\text{PORESET}}$: MODCK1/BNKSEL(0)/TC(0) as BKSEL0 MODCK2/BNKSEL(1)/TC(1) as BKSEL1 MODCK3/BNKSEL(2)/TC(2) as BKSEL2		

Table 4-2 MSC8101 Hard Reset Configuration Word (HCW1)

Field	*Data Bus Bits*	*Prog Value [Bin]*	*Implication*	*Offset In HCW source [Hex]*	*Value [Hex]*
BC1PC	24:25	’00’	**Buffer control** 1-pin configuration BCTL1/ DBG_DIS functions as BCTL1	18	1E
Reserved	26	’0’	**Reserved.** Should be cleared.		
DLLDIS	27	’1’	**DLL off**		
MODCK_H[a]	28:30	‘111’	**High-order bits of the MODCK.** Clock configuration scheme 57 for MSC8101		
Reserved	31	’0’	Reserved. Should be cleared.		

a. Applied only once after power-up reset.

4.2.7 Slave Reset Configuration

The primary h/w setting, using two DIP Switches, will configure the MSC8102 after power-up. The following modes are available:

- System Mode - the configuration word is fetched and boot is achieved via the system bus in the master mode (DIP Switch SW4/3 is in “SYS” position).
- DSI Mode - configuration word is written by host; boot is completed via the system bus in the Slave mode (DIP Switch SW4/3 in “DSI” position).
- DSI bus width of either 64-bit or 32-bit is chosen by the DIP Switch SW7/3.

See *Table 4-3 "MSC8102 Pins Dependant upon Power-on-Reset Configuration" on page 46* for further details.

The MSC8102 may be reconfiged on demand when the Host processor programs the BCSR register with the desired configuration setting and invokes a Power-on-Reset or Hard Reset sequence for the MSC8102. This setting is called a secondary reset configuration. MSC8102 Hard Reset configuration may also be achieved manually by pressing the Hard Reset Push button

(HRESETs). See *Figure 4-2 "Secondary Reset Configuration Details"* below.

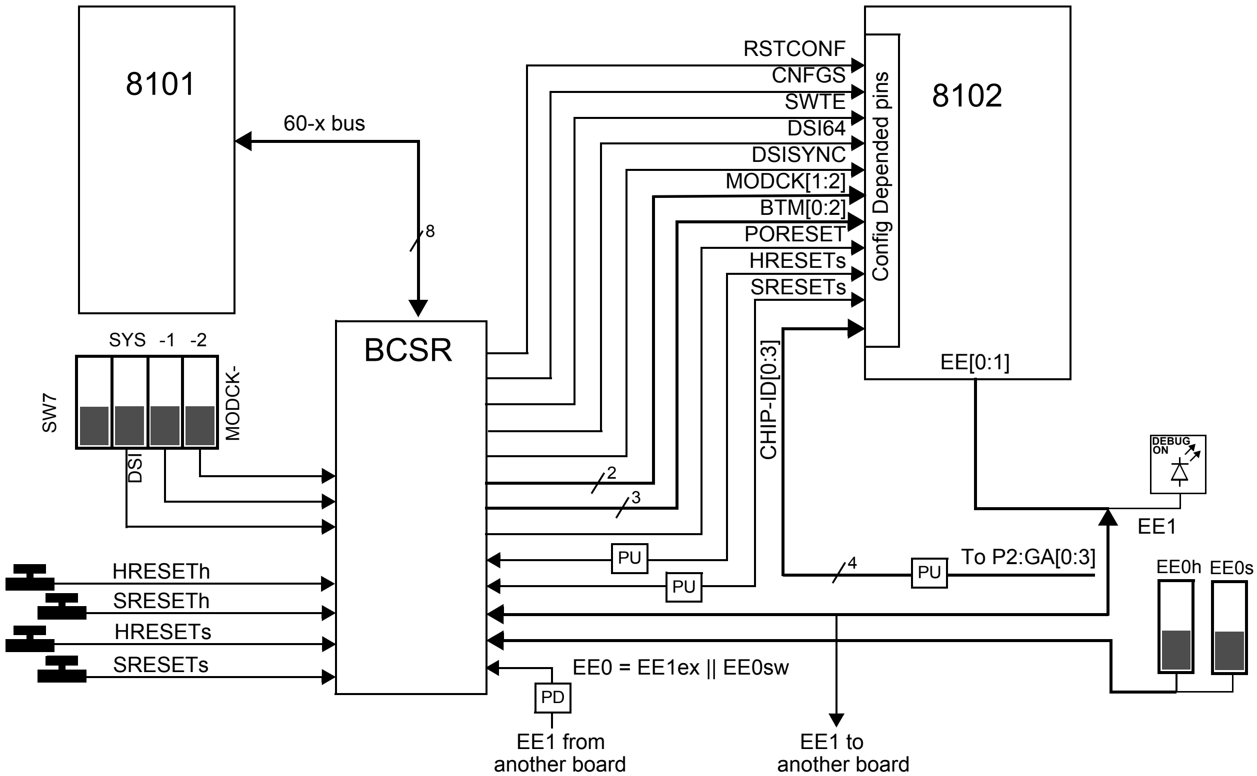


Figure 4-2 Secondary Reset Configuration Details

Note the MSC8102 Reset configuration setting found below. The MSC8102 Reset configuration may be loaded in two ways. Either by the Host or, depending upon the DSI or SYS mode, taken from the device connected to the CS0 of the MSC8102 System bus (Slave-side Flash).

Table 4-3 MSC8102 Pins Dependant upon Power-on-Reset Configuration

Name of signal	*Value sampled at pins*	*Primary Mode*	*Implementation*
MODCK[1–2]	‘00’ or ‘01’	Clock mode 0 or clock mode 1.	DIP Switch SW4/1-2 primary setting or driven by the BCSR for secondary setting.
$\overline{\text{RSTCONF}}$	‘0’	Configuration Master from the System or DSI bus.	DIP Switch setting
CNFGS	‘0’	Configuration Master from the System bus.	
	‘1’	Configuration Master from the DSI bus.	
SWTE	‘0’	Software Watchdog Timer Disable	Set logically if DSI is config master.
	‘1’	Software Watchdog Timer Enable	Set logically if System Bus is config master.

BTM[0:2]	‘000’	Boot from the 60-x bus	Configuration modes controlled by DIP Switch SW4/3 setting.
	‘001’	Boot from the DSI	
DSI64	‘0’ or ‘1’	32-bit DSI data bus with 64-bit System data bus or visa versa.	Controlled by DIP Switch SW7/3.
DSISYNC	‘0’	DSI set in Asynchronous mode	Pulled-down permanently.
CHIP_ID[0–3]	‘1111’	Chip ID encoded to ‘0xF’	Pulled-up permanently. Prepared for backplane application. For multi-chip (multi-board) system, ID will be set according to slot’s GA (geographic address).

Table 4-4 MSC8102 Hard Reset Configuration Word (HCW2)

Field	*Data Bus Bits*	*Prog Value [Bin]*	*Implication*	*Offset In HCW for system source*[a]	*Value [Hex]*
EARB	0	’0’	Internal **Arbitration** selected.	0	24
EXMC	1	’0’	Internal **Memory Controller.** CS0 active at system boot.		
INTOUT	2	’1’	**INT_OUT** function is active.		
EBM	3	’0’	Single **chip bus mode** is assumed.		
BPS	4:5	’01’	8-bit **Boot Port Size** for the Slave Flash memory.		
SCDIS	6	’0’	**SC140** enabled.		
ISPS	7	‘0’	**Internal space port size** for ext. master access is 64-bit. Not an issue as this feature is not supported in the current board configuration.		
IRPC	8	’0’	**Interrupt pin configuration.** BADDR(29)/IRQ5, BADDR(30)/IRQ2, BADDR(31)/IRQ3 are selected as interrupt pins.	8	20
Reserved	9	‘0’	**Reserved.** Must be cleared		
DPPC	10:11	‘10’	**Data Parity Pin configuration.** NC/DP0/DREQ1/EXT_BR2, IRQ1/DP1/DACK1/EXT_BG2, IRQ2/DP2/DACK2/ EXT_DBG2, IRQ3/DP3/DREQ2/ EXT_BR3, IRQ4/DP4/DACK3/ EXT_BG3, IRQ5/DP5/DACK4/EXT_DBG3, IRQ6/DP6/DREQ3, IRQ7/DP7/DREQ4 are selected as DMA pins: DREQ1, DACK1, DACK2, DREQ2, DACK3, DACK4, DREQ3, DREQ4.		
NMIOUT	12	’0’	**NMI interrupt** is serviced by the core.		
ISBSEL	13:15	’000’	IMMR initial value 0xF000_0000. i.e., **the internal space** initially resides at this address.		

Table 4-4 MSC8102 Hard Reset Configuration Word (HCW2)

Field	*Data Bus Bits*	*Prog Value [Bin]*	*Implication*	*Offset In HCW for system source[a]*	*Value [Hex]*
Reserved	16	’0’	**Reserved.** Non-functional cleared bit.	10	26
BBD	17	’0’	**Bus busy** pins set as: ABB/IRQ4 pin is ABB DBB/IRQ5 pin is DBB.		
MMR	18	‘1’	**External Bus Request masked.**		
Reserved	19	‘0’	**Reserved.** Must be cleared.		
TTPC	20	‘0’	**Transfer Type Pin Configuration.** TT[0]/NC, TT[2]/CS5, TT[3]/CS6, TT[4]/CS7 are chosen as transfer type pins: TT[0], TT[2], TT[3], TT[4].		
CS5PC	21	‘1’	**Chip Select 5 Pin Configuration.** CS5/ BCTL1 pin is configured as BCTL1.		
TCPC	22:23	’10’	**Transfer code** pins are configured after PORESET: TC0/GPIO0/ BNKSEL0 as BNKSEL0 TC1/GPIO1/ BNKSEL1 as BNKSEL1 TC2/GPIO2/ BNKSEL2 as BNKSEL2		
LTLEND	24	‘0’	Defines the Host **Endian mode** as Big Endian.	18	14
PPCLE	25	’0’	**PowerPC Little Endian Mode.** Unimportant while the Host is Big Endian (bit LTLEND is zero).		
Reserved	26	’0’	**Reserved.** Should be cleared.		
DLLDIS	27	’1’	**DLL off**.		
MODCK_H[b]	28:30	‘010’	**High-order bits 3:5 of the MODCK.** Default Clock mode is 11.		
Reserved	31	’0’	**Reserved.** Should be cleared.		

a. For the DSI source a 32-bit Configuration Word is written at offset 0x261BE050
b. Applies only ONCE after power-up reset.

4.3 Clock Source

4.3.1 Host Main Clock Scheme

MSC8101 requires a single clock source for the main clock oscillator. The 55MHz@3.3V clock oscillator is mounted on the 8-pin DIP socket (half-size form factor) for ease of replacement. All MSC8101 60-x bus timings are referenced to the DSP output clock. CLKOUT is driven to a zero delay buffer in order to split the load between the clock consumers on the board. One channel is relegated to the MSC8101 DLL input in order to eliminate wire propagation delay to the SDRAM devices.

An optional pulldown resistor is capable of transforming the Clock Zero Delay (ZD) Buffer into

a regular clock buffer when the internal PLL is disabled. In such a case the typical propagation delay of the clock buffer may reach 7ns.

If the ADS is set with the ZD Buffer as default, then the MSC8101 must be configured with DLL-off. See HCW1 in Table 2-2. On the other hand, if the ZD Buffer is disabled (clock buffer mode) then the MSC8101 must be configured with DLL-on in order to function properly with SDRAM.

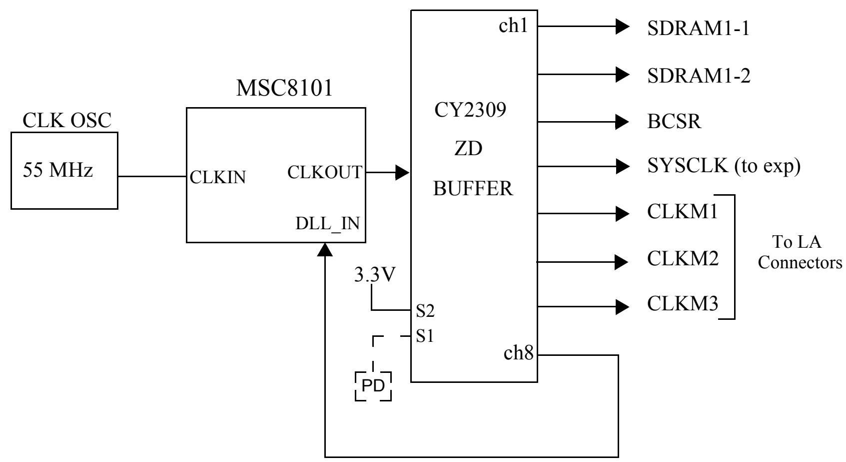


Figure 4-3 Host Clock Distribution Scheme

4.3.2 Slave Main Clock Scheme

MSC8102 requires a single clock source for the main clock oscillator. For ease of replacement the 41.6MHz @3.3V clock oscillator is mounted on the 8-pin DIP socket (half-size form factor). All MSC8102 system bus timings are referenced to the DSP output clock. CLKOUT is driven to a ZD Buffer in order to split the load between the clock consumers on the board. One channel reaches the MSC8102 DLL input in order to eliminate wire propagation delay to the SDRAM device.

An optional pulldown resistor is capable of transforming the ZD Buffer into a regular clock buffer when the internal PLL is disabled. In such a case the typical propagation delay may reach up to 7ns.

If the ADS is set with the ZD Buffer as default, then the MSC8102 must be configured with DLL-off. See HCW2 in Table 2-4.   On the other hand, if the ZD Buffer is disabled (clock buffer mode)

then the MSC8102 must be configured with DLL-on in order to function properly with the SDRAM.

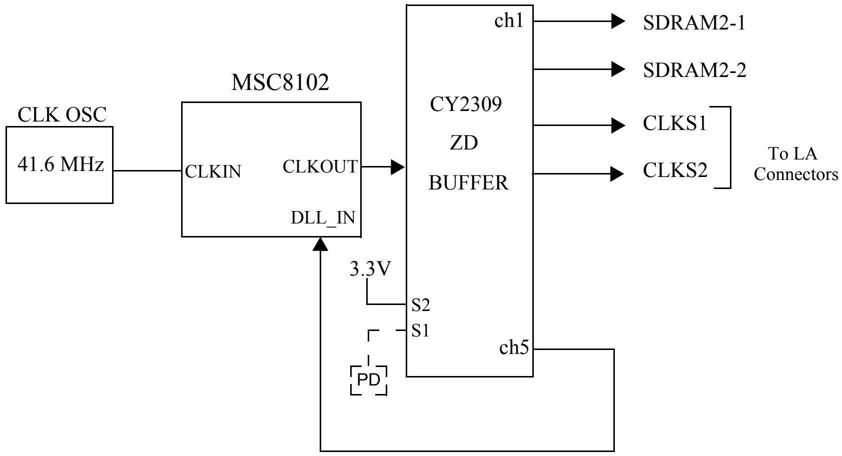


Figure 4-4 Slave Clock Distribution Scheme

4.4 60-x Bus Buffering and Muxing

In order for the 60-x bus to achieve peak performance, it's capacitive load must be reduced as much as possible. As a consequence the slower devices on the bus (i.e. the Flash, ATM SONET Framer M/P interface, BCSR and external tool bus) are buffered while the SDRAM devices and the MSC8102 DSI side are not buffered.

Buffers are provided over address and, where necessary, strobe lines. The buffers used are from the 74LVC family (by Texas Instruments) which operate on 3.3V although are 5V tolerant[A]. All the expansion bus lines (64bit data @29 address lines + strobes) are also buffered. In order to reduce noise and reflections, serial damping resistors are added to selected MSC8101/MSC8102 strobe lines.

Transceivers are provided for data and are only open under two conditions - when access to a valid[B] buffered board address exists or during a Hard Reset configuration sequence[C]. For example, data conflicts are avoided when unbuffered or off-board memory is read, provided it is not mapped to a valid board address. The user can avoid such errors through correct programming of the Memory Controller.

The MSC8102 DSI bus provides additional configuration options in the form of different sized data buses: 64-bit or 32-bit. The ADS is configured by the DIP Switch SW7/3 that sets the system bus to 64-bit (SYS64 position) and the DSI bus to 32-bit. The opposite configuration, also using the DIP Switch SW7/3 setting, pertains to data bus width distribution: system bus at 32-bit and DSI bus at 64-bit. See *Table 1-1 "The ADS Switches" on page 15*. To achieve this connectivity a bus switch device is utilized. See *Figure 4-5* below:

A. Required for Flash and BCSR
B. An address which is covered in a Chip-Select region, that controls a buffered device by BCSR logic.
C. To enable activation of a configuration word stored in the Flash memory or BCSR.

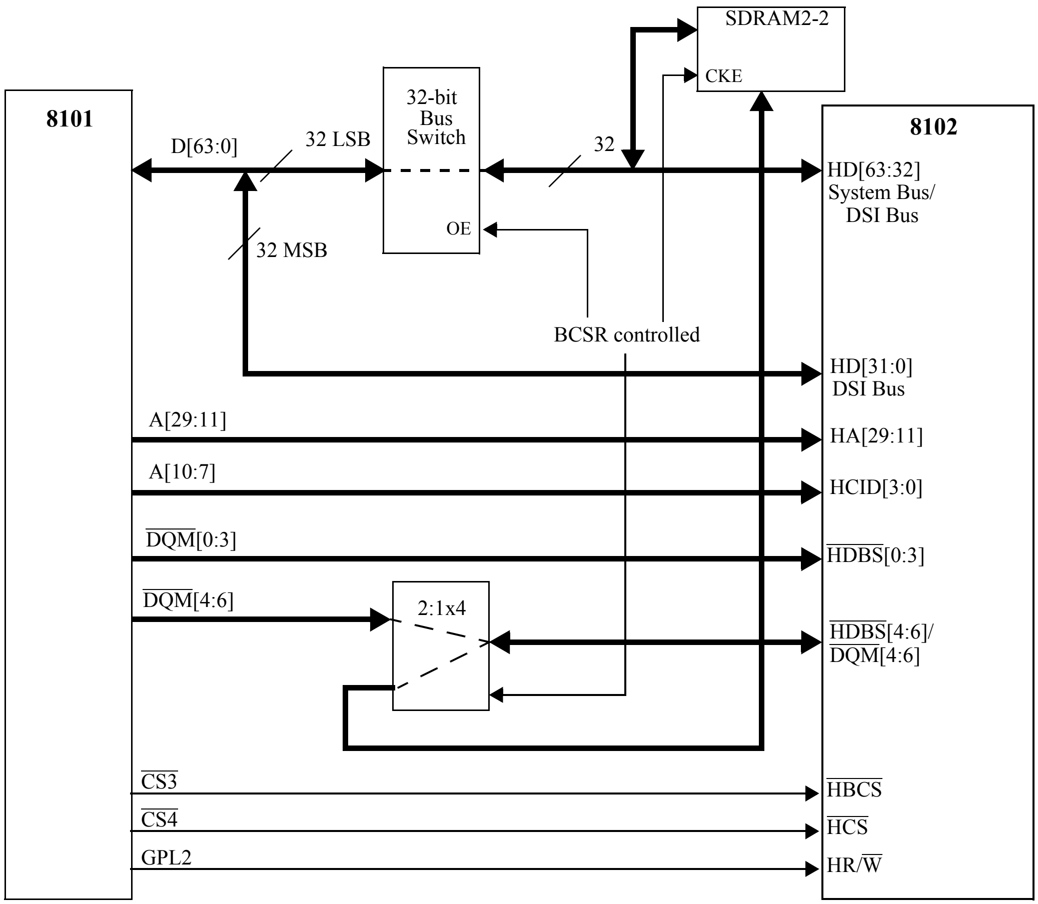


Figure 4-5 DSI Bus to 60-x Bus Connection

4.5 Chip Select Designation

The MSC8101/MSC8102 Memory Controller is used as a chip-select generator in order to access on-board memory. The same functionality applies in the case of off-board memory, however, in this instance access is achieved via J1/J2 expansion connectors. Consequences of this usage are board area reduction, cost reduction, better power consumption and increased flexibility.

Instances exist when a Chip Select (CS) region, assigned to a buffered[A] memory, is disabled via the BCSR. This is undertaken so that local data transceivers are disabled when accessing a given CS region and, consequently, possible[B] contention over data lines is avoided. CompactPCI® expansion connectors J1/J2 carry lines of Memory Controller that are used for accessing ADSs boards mounted on the peripheral slots of a CompactPCI® 6U backplane. This, as opposed to the ADS board, that is present on the CompactPCI® 6U backplane system slot. The above noted system configurations incorporate ADS and ADSs board connections and thus illustrates the MSC8102 DSP-farm application when the MSC8101 acts as a host micro controller.

MSC8101 CS assignments for various MSC8102ADS memory/registers are outlined in *Table*

A. Buffers do not open when an unbuffered CS region is accessed.
B. During read cycles.

4-5 "Host Memory Controller Assignment".

Table 4-5 Host Memory Controller Assignment

MSC8101 Chip Select	*Location*	*Assignment*	*Bus*	*Timing Machine*
CS0	External	Flash, BCSR Config Word	60-x (Buffered)	GPCM
CS1	External	BCSR	60-x (Buffered)	GPCM
CS2	External	SDRAM1 bank	60-x (Unbuffered)	SDRAM Machine
CS3	External	HBCS(DSI broadcast)	60-x (Buffered+XBuffered)	GPCM
CS4	External	HCS(DSI select from 0 to 15)	60-x (Buffered+XBuffered)	UPMA
CS5	External	ATM SONET Framer Microprocessor I/F	60-x (Buffered)	UPMB
CS6	External	For off-board application.	60-x (XBuffered)	GPCM/UPMx(A or B)
CS7		Not supported on the ADS.	-	-
CS10	Internal	DSPRAM	Local PPC	UPMC
CS11	Internal	DSP Peripherals	Local PPC	GPCM

Table 4-6 Slave Memory Controller Assignment

8102 Chip Select	*Location*	*Assignment*	*Bus*	*Timing Machine*
CS0	External	Flash/BCSR Config Word[a]	60-x (Buffered)	GPCM
CS1	External	Not used/BCSR[a]	60-x (Buffered)	GPCM
CS2	External	SDRAM2 bank	60-x (Unbuffered)	SDRAM Machine
CS3	External	TSI	60-x (Buffered)	UPMA
CS4	External	FALC T1/E1	60-x (Buffered)	UPMA
CS5-7	External	Not supported on the ADS.	-	-
CS9	Internal	IP bus	Local PPC	GPCM
CS10	Internal	EFCOP	Local PPC	GPCM
CS11	Internal	L1's & L2 Memory	Local PPC	UPMC

a. The BCSR function is only supported for ADSs board configurations.

4.6 Local Interrupter

4.6.1 Host-side

External interrupts exist that are applied to the MSC8101:

1) A specific-usage push button provides the source of the ABORT (NMI) signal.
2) The Slave MSC8102 (INT_OUT) interrupt receives over line $\overline{\text{IRQ1}}$.
3) The ATM SONET Framer interrupt receives over line $\overline{\text{IRQ6}}$.
4) Available off-board interrupt sources from ADSs boards include lines $\overline{\text{IRQ2}}$ to $\overline{\text{IRQ4}}$.
5) Ready/Busy Status of FLASH received over line $\overline{\text{IRQ7}}$.

4.6.2 ABORT Interrupt to MSC8101

ABORT (NMI) is manually push-button generated. When the button is pressed, $\overline{\text{IRQ0}}$ input is asserted to the MSC8101. This type of interrupt is intended to support any resident debugger usage made available to the MSC8102ADS.

4.6.3 Slave Interrupt

On-board Slave Interrupt Controller output is served by the Host interrupt, $\overline{\text{IRQ1}}$. MSC8101 processor interrupt lines, $\overline{\text{IRQ2}}$ to $\overline{\text{IRQ4}}$, may be used to support up to three optional ADSs boards.

4.6.4 ATM SONET Framer Interrupt

Interrupt support of the ATM SONET Framer event report is achieved by connecting the interrupt output of the U30 ATM SONET Framer ($\overline{\text{INT}}$) to the $\overline{\text{IRQ6}}$ line of the MSC8101.

4.6.5 Flash Ready Interrupt

Output from the Ready/Busy Flash open-drain pin indicates whether a program/erase Embedded Algorithm is still in progress or has been completed. Tying this output to interrupt line

$\overline{IRQ7}$ allows for the simplification of the burning program that services Flash.

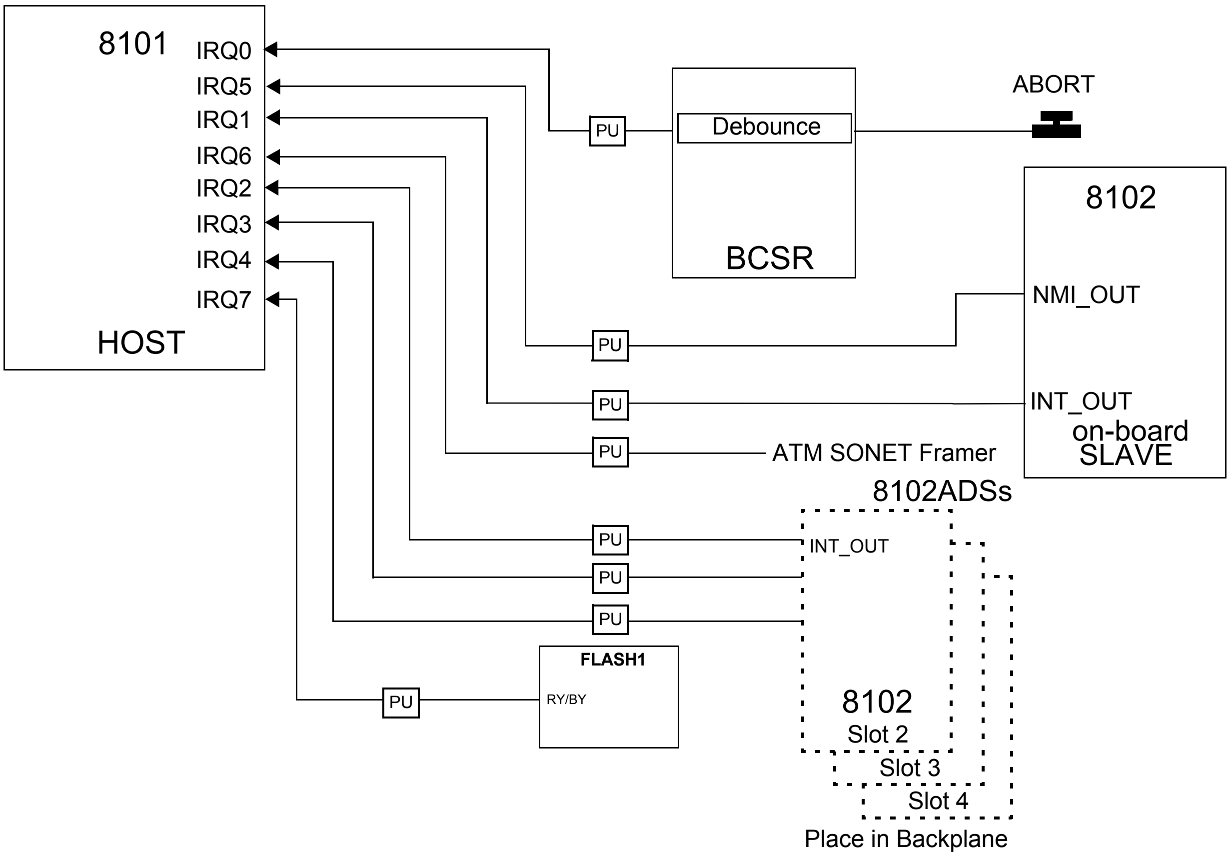


Figure 4-6 Host Interrupt Utilization Diagram

4.6.6 Slave-side

Noted below are external interrupts applied to the MSC8102:

1) A specific-usage push button provides the source of the ABORT (NMI) signal.
2) TSI interrupt receives over line $\overline{IRQ2}$ muxed with line BADDR31.
3) FALC56 interrupt receives over line $\overline{IRQ3}$ muxed with line BADDR30.
4) Ready/Busy Status of FLASH received over line $\overline{IRQ1}$.

4.6.7 ABORT Interrupt to MSC8102

ABORT (NMI) is manually push-button generated. When the button is pressed, $\overline{IRQ0}$ input is asserted to the MSC8102. This type of interrupt is intended to support any resident debugger usage made available to the MSC8102ADS.

4.6.8 TSI Interrupt

The TSI interrupt request originates from $\overline{IREQ}$ output of Infineon's SWITI device. The SWITI

device has been configured as an open-drain and will be driven over line $\overline{\text{IRQ2}}$.

4.6.9 FALC56 Interrupt

E1/T1 Framer (FALC56) interrupts are served by $\overline{\text{IRQ3}}$. In this case the FALC56 has been configured as an open-drain output.

4.6.10 Flash Ready Interrupt

Output from the Ready/Busy Flash open-drain pin indicates whether a program/erase Embedded Algorithm is still in progress or has been completed. Tying this output to interrupt line $\overline{\text{IRQ1}}$ allows for the simplification of the burning program that services Flash.

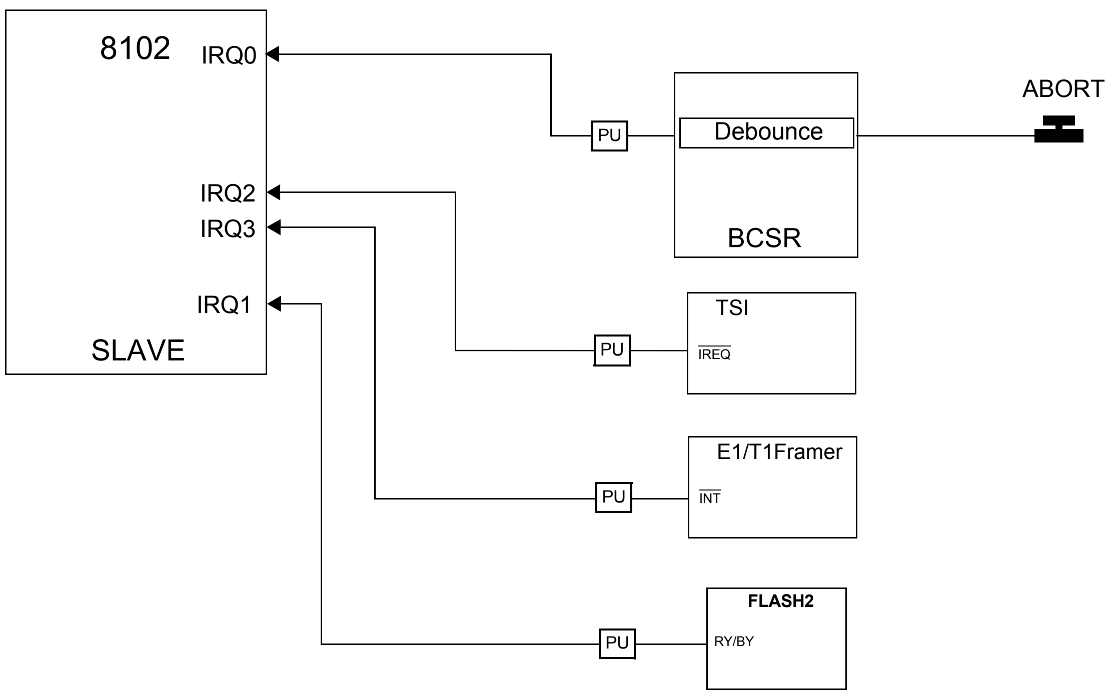


Figure 4-7 Slave Interrupt Utilization Diagram

4.7 SDRAM

On the Host-side of the ADS is an unbuffered SDRAM bank that includes two Micron devices with a total size of 16MB@64-bit.

The MSC8102 System Bus is powered by a SDRAM bank that includes the same two devices found on the Host-side. The SDRAM bank may be configured at 16MB@64-bit with two SDRAM parts for a full-width System Bus or at 8MB@32-bit with one SDRAM part for a half-size System Bus. The SDRAM configuration feature is supported by BCSR logic that controls an address bus mux device. The bus mux provides address line shifting as shown below in "".

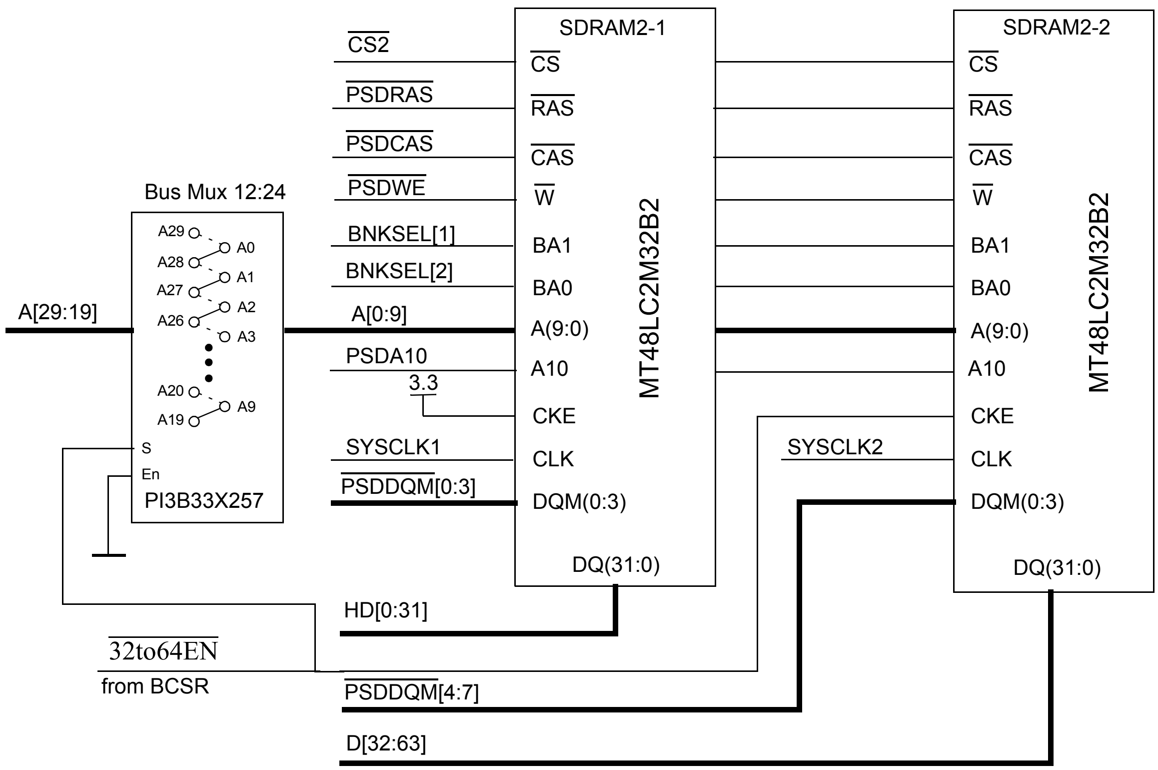


Figure 4-8 SDRAM Slave-side Connection Diagram

4.7.1 SDRAM Programming

In order to establish its mode of operation the SDRAM is, after power-up, initialized by means of programming. The SDRAM is programmed by issuing a Mode Register Set command wherein command data is passed to the Mode Register via the SDRAM's address lines. The Mode Register Set command is fully supported by the MSC8101/MSC8102 SDRAM machine.

The Mode Register programming value for Micron's SDRAM MT48LC2M32B2-8 is noted below in *Table 4-7 "SDRAM Mode Register Programming up to 100 MHz"*.:

Table 4-7 SDRAM Mode Register Programming up to 100 MHz

SDRAM Address Line[a]	*SDRAM Mode Reg Field*	*Value*	*Description*
A10	Reserved	'0'	Must program to zero
A9	WB (Write Burst Mode)	'0'	Write Burst enabled
A8, A7	Operating Mode	'00'	Standard Operation (default)
A6 - A4	CAS Latency	'010' or '011'	Program 2 or 3 CAS Latency depending on Bus frequency
A3	Burst Type	'0'	Sequential Burst Access
A2 - A0 (LSB)	Burst Length	'010'/'011'[b]	4/8 Word Burst Length (Beat count)

a. In effect the SDRAM2-1 A0 will be connected to the MSC8102 A29/A28 address line (32/64 -bit System bus width mode).
b. An 8-beat burst is programmed for the MSC8102 32-bit System Bus width.

4.7.2 SDRAM Refresh

SDRAM has an auto-refresh mode. For example, when using the first SDRAM Machine's periodic timer, an auto-refresh command is issued to the SDRAM every 15 μsec. Consequently all 4096[A] SDRAM rows are refreshed within spec'd 61.44 msec. The 2.56 msec interval of refresh redundancy within the (spec'd 61.44 msec) window acts as a safety measure covering, for the refresh controller, possible delays in bus availability.

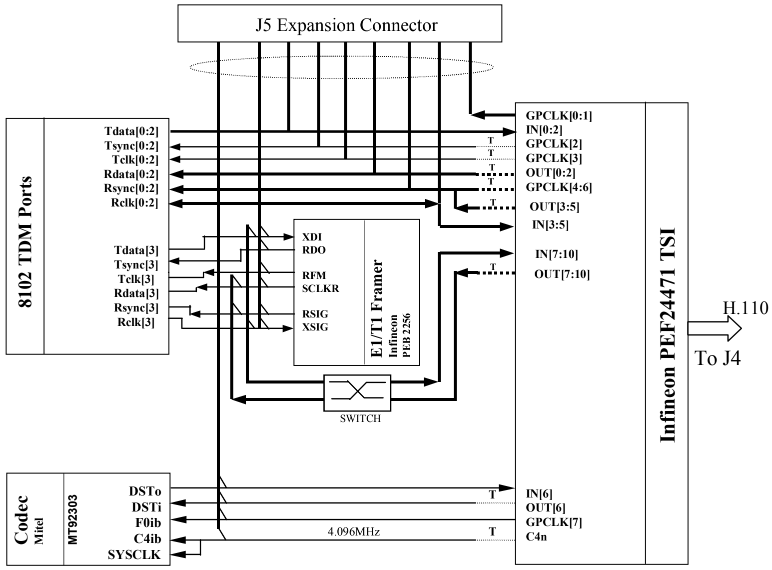
4.8 Flash

MSC8102ADS will support the AMD flash device, Am29LV320 4MB volume. The Host-side Flash is interfaced to a 16-bit buffered 60-x bus. The same Flash device type, found on the Slave-side, is configured by the hardware to an 8-bit mode. The Hardware Write Protect pin, found in both the Host and Slave -side Flashes, is driven by BCSR logic and provides improved protection against the accidental erasing of both the HCW and of the base boot code stored in the boot sector.

4.9 TDM Port Peripherals

Four MSC8102 TDM ports interface with the Infineon PEF24471 Time-Slot Interchanger. In order to make the testability and flexibility features accessible to varying modes, all the TDM lines go to expansion connector J5 of CompactPCI®. Note the general interconnection diagram *Figure 4-9* below. Four MSC8102 TDM ports interface with the Infineon PEF24471 Time-Slot Interchanger. In order to make the testability and flexibility features accessible to varying modes, all the TDM lines go to expansion connector J5 of CompactPCI®. Note the general interconnection diagram and *Figure 4-10 "TDM Clocking Diagram"*, below.

A. Each SDRAM component is composed of 4 internal banks each with 4096 rows. They are refreshed in parallel.



"T" denotes the capability of setting output Hi-Z in order to drive a signal from an external source

Figure 4-9 TDM Connection Diagram

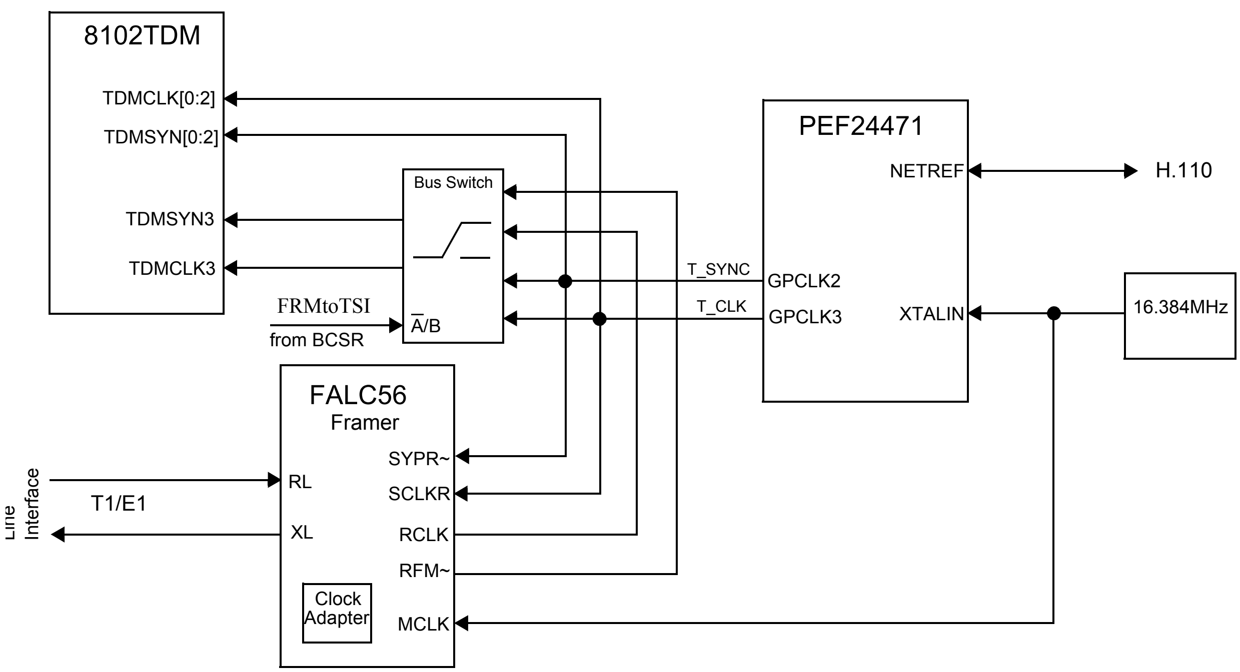


Figure 4-10 TDM Clocking Diagram

Figure 4-10 "TDM Clocking Diagram", above, depicts variant clocking configurations.

The clock/sync has several modes. The first mode is an internal clock master based on the 16MHz clock oscillator's source for all four TDM ports. The second denotes the T1/E1 network master mode as provided for the third TDM port by the FALC56 E1/T1 Framer. The last available clocking mode is a Slave to the CT-bus Master Clock's synchronization of the Time Slot Interchanger (TSI) device.

4.9.1 Time Slot Interchanger (TSI)

The PEF24471 TSI device utilized on the ADS is a member of the SWITI family. It provides a complete time slot switch and interface for the H.110 time division multiplexed (TDM) buses. The PEF24471 TSI device can switch between local input and output buses as well as switch between the H.110 bus and the local bus. The PEF24471 has a capacity of up to 2048 connections.

As well as supporting the newer H-MVIP and ECTF H. 1x0 standards, the TSI chip is backward compatible to bus standards MVIP-90 and Dialogic's SC - Bus. Local streams may operate on 16 physical inputs and outputs. The data rates are programmable on each of the 32 physical streams - the streams are selected in groups of four. The data rates are on a per stream basis as follows: 2.048 Mbits/s and 4.096 Mbits/s or 8.192 Mbits/s and 16.384 Mbits/s.

After buffering, the PEF24471 device interfaces at 8-bit to the MSC8102 System bus.

To view the program manual see *[3]*.

4.9.2 E1/T1 Framer

Infineon's FALC®56 Framer PEB 2256 supports one network line as well as containing analog and digital function blocks configured and controlled by the MSC8102 Slave-side processor. The FALC®56 Framer PEB 2256 has a multitude of implemented functions. As a consequence it is suited to a wide range of networking applications and, further, fulfills all required interfacing between analog E1/T1/J1 lines and the digital PCM system highway. See the connection schemes found in *Figure 4-9 "TDM Connection Diagram"*.

4.9.3 CODEC

The ADS uses the Mitel MT92303 Dual CODEC to provide complete audio to the PCM interfaces - including filtering and optional data "companding" as required by the ITU-T G.711 & G.712 recommendations. Two built-in amplifiers allow direct connection to a handset, headset, auxiliary channel and microphone/speaker.

Three PCM Data Formats are available: 16-bit Linear; "companded" ITU-T A-law; and μ-law. PCM data is transferred via a serial interface operating in the ST-bus mode. Though serial I/F is programmed to an ST-bus mode, it is available for allocating data to any of the 32 available channels and is easily interfaced to the local channel of the TSI device.

CODEC control and programming occur over a serial interface implemented by two MSC8102 GPIO's and a CS pin. CS control is realized via the BCSR register bit. One GPIO functions as a

clock while the other acts as a bi-directional data path.

Table 4-8 CODEC Initialization

Byte address of dual Codec in hex	*Byte Name*	*Value in hex*		*Function*	*Action*
		Operation Mode	*Test Mode*		
0,1	Control Register	‘01’	‘03’	Test: only Rx Enable or together with Sidetone. PCM set in Linear mode. A-Law.	Should be set
2,3	CODEC Enable	‘01’		CODEC enable, gain is 0dB.	Should be set
4,5	Rx Hi-Pass-Filter	‘00’		Cut Off Frequency of RX Path ‘DSP’ Hi Pass Filter is 0dB.	Accept power-up setting
6,7	Sidetone Gain	‘00’	‘0D’	Sidetone gain - 39dB for operation mode or 0dB for test mode.	Dependent setting
8,9	DSP Test	‘00’	‘01’	Digital side loopback for test mode.	Dependent setting
0A,0B	Tx Gain	‘0’		Tx gain is 0dB.	Accept power-up setting
0C	Audio Interface for Auxtone	‘CF’		AUXTONE gain is 0dB, Electret Microphone Bias is 2.0V.	Should be set
0D-0F	Audio Interface for three channels	‘CE’		Rx gain is 0dB, Electret Microphone Bias is 2.0V.	Should be set
10	Audio Interface Enable	‘73’		Enable Audio interface 0 and 1, Voltage Reference and two Tx Analog circuitry.	Should be set
11	Cross-Point Selection	‘34’		Route CODEC 0 to Audio Interface 0 and CODEC 1 to Audio Interface 1.	Should be set
12	Codec Channel Allocation	‘00’		CODEC 0 allocates on channel 0 of ST-bus.	Accept power-up setting
13	Codec Channel Allocation	‘01’		CODEC 1 allocates on channel 1 of ST-bus.	Should be set
14	Status Channel Allocation	‘02’		Status allocates on channel 2 of ST-bus.	Should be set
15	General Mode Control	‘00’		Select ST-bus, Microphone path Enable.	Accept power-up setting
16	System Clock	‘0D’		Select System Clock 4.096 MHz (as well as ST-bus clock), PLL enable.	Should be set
17,18	Test Registers	-		Testing reserved for the manufacturer.	-
19	Status Register	-		Read only.	-

4.10 RS232 Transceivers

Two MSC8102ADS RS232 ports are connected to the following: the MSC8101 Host-side processor SCC1 port; and, the Slave-side UART port. The port connections assist in user applications and, further, provide convenient communication channels for both the terminal and host computer.

Using a lone 3.3V single power supply with disable mode, the MAXIM MAX3241 Transceiver internally generates RS232 levels during which receive buffers are tri-stated. When asserting (low) the RS232_EN1 or RS232_EN2 bits in BCSR1/6-7, the corresponding transceiver is enabled. When negated the receiver outputs are tri-stated and the corresponding transceiver is disabled. For off-board applications it is possible to use Slave-side UART port signals via the J5 expansion connector.

The 9-pin female D-Type RS232 connectors are configured to be directly connected (via a flat cable) to a standard IBM-PC-like RS232 connector. Note the below figures, *Figure 4-11* and *Figure 4-12*, that illustrate the RS232 connector pinouts where the directions “I”, “O” are relative to the MSC8102ADS board. For example, “I” means input to the MSC8102ADS.

The Host-side RS232 port provides expanded serial I/F including h/w flow control support.

The Slave-side UART port is intended for null-modem connectivity.

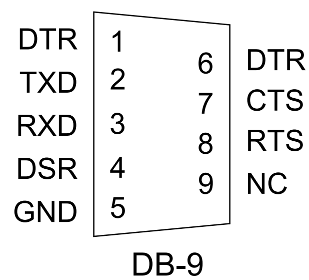


Figure 4-11 Host RS232 Serial Port Connector

- DTR - Data Terminal Ready. This line is always asserted by the MSC8102ADS. (O)
- TXD - Transmit Data (O)
- RXD - Receive Data (I)
- DSR - Data Set Ready (I)
- CTS - Clear To Send (I)
- RTS - Request To Send (O)

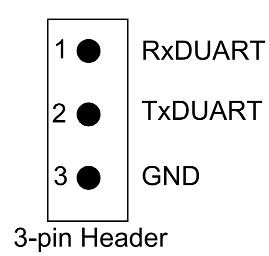


Figure 4-12 Slave UART Serial Port Connector

- RxDUART - Receive Data (I)
- TxDUART - Transmit Data (O)

4.11 Packet Peripherals (Host-side)

4.11.1 ATM SONET Framer

MSC8101 ATM controller support is provided by an on-board 155.52 Mbps ATM Framer connected via UTOPIA-8 I/F to the FCC1 of the MSC8101. It is used in conjunction with PMC-Sierra's PM5384.

The Framer is controlled by the transceiver's microprocessor I/F. The buffered microprocessor I/F is configured by the MSC8101 memory controller in Memory Controller General Purpose Chip-select Machine (GPCM) mode. The Framer has a 3.3V power supply and connects directly to the MSC8101's CPM port.

ATM Framer reset input is driven by the MSC8101's $\overline{\text{HRESET}}$ signal and, as such, reset occurs whenever a Hard Reset sequence is performed. The ATM Framer may be reset by either asserting ATM_RST bit in BCSR1/3 or by a sw controlled internal register.

ATM Framer transmit and receive clocks are fed by a 19.44 MHz +/- 20 ppm clock generator powered by 3.3V power supply. MSC8101 provides the receive and transmit FIFO clock - either from the same or a separate hard-configured clock.

The ATM SAR is connected by an optical I/F to the physical medium. HP's HFBR 5805 optical I/F, operating at 1300 nm with up to a 2 km transmission range, is used.

4.11.2 10/100 T-Base Ethernet Phy

A Fast Ethernet port with T.P. (100-Base-TX) I/F is provided on the MSC8102ADS. The port also supports 10 Mbps Ethernet (10-Base-T) via the LSI LS80225 Transceiver.

LS80225 operates from a single 3.3V power supply and connects directly to the FCC2 port of the MSC8101 via the MII interface. The interface is used for both device control and data path. The initial LS80225 configuration is achieved by setting the MII control port to address "0".

LS80225 reset input is driven by MSC8101's $\overline{\text{HRESET}}$ signal. The transceiver is reset whenever a Hard Reset sequence is undertaken. The Phy is able to interrupt the MSC8101 via the $\overline{\text{IRQ7}}$ line.

4.12 Board Control & Status Register - BCSR

The BCSR, an 8-bit wide read / write register file, controls or monitors most of the ADS hardware options. For the full ADS board configuration the BCSR resides on the Host 60-x bus. In the case of the ADSs board configuration, the BCSR is interfaced to the MSC8102's System Bus. The BCSR includes 6 registers, BCSR0 to BCSR5. The BCSR6 - BCSR7 slices are not implemented.

BCSR0 to BCSR6 are duplicated numerous times within a CS region. This is due to the CS region's 32KB minimum block size and the fact that only address lines A[29:31] are decoded for register selection by the BCSR. BCSR is implemented on a PLD Altera device that provides register and logic functions over some ADS signals. See *Table 2-1 "MSC8102ADS Specifica-*

tions" on page 20.

The BCSR controls or monitors the following functions:

1) Power-on-Reset configuration setting for the Slave-side.
2) Hard Reset for Host and up to four Slaves (three of which are ADSs off-board Slaves).
3) Soft Reset for Host and an on-board Slave.
4) Hardware Reset for the following devices:
    - T1/E1 Framer FALC56
    - Fast Ethernet Phy
    - ATM Framer
    - TSI device
5) RS232 (Host and Slave) Enable / Disable port.
6) CODEC Enable and Reset device is found on the serial control port.
7) BCSR provides FLASH (Host and Slave) devices with h/w boot protection.
8) BCSR provides TDM port # 3 with muxing between the E1/T1 Framer and the TSI device.
9) Two Host LEDs (one green, one red) provide s/w signaling.
10) Two Slave LEDs (one green, one red) provide s/w signaling.
11) Secondary Power-On-Reset Control for the MSC8102 exists.
12) ADS has special function support for MSC8102 (test functions register).
13) Status register includes:
    - Software Option Identification (set by DIP SW5 Switch)
    - ADS Configuration code
    - ADS Revision code
    - BCSR Revision code

Sections of the BCSR slice control registers generally have low active notations. This means that a bit function will be realized while the bit is zero. When a bit is set to “1” a related function is disabled. The default setting is assumed to be non-functional.

4.12.1 BCSR0 - Board Control / Status Register 0

The BCSR0 serves as a control register on the ADS and, although it only resides over D(0:7) lines of the 60-x data bus, it is accessed from the BCSR base address as a **byte** at **offset 0x0**. The BCSR0 may be read or written at any time. BCSR0 defaults are attributed at the time of main Power-On-Reset or HRESETh. BCSR0 fields are described below in *Table 4-9 "BCSR0 Description"*:

Table 4-9 BCSR0 Description

BIT	*MNEMONIC*	*Function*	*DEF*	*ATT.*
0	FLASHPRT1	***Flash 1 h/w Protection.*** HCW and boot code, found in the Flash boot sector, are protected in the Host-side Flash when the FLASHPRT1 is asserted (**low**). To unprotect the Flash boot sector, reset unlock bit FLUNLCK1 at BCSR6.0 and then write **high** in the FLASHPRT1 bit. This allows for further erase/write operations in the boot sector.	0	R,W

Table 4-9 BCSR0 Description

BIT	MNEMONIC	Function	DEF	ATT.
1	FLASHPRT2	***Flash 2 h/w Protection.*** HCW and boot code, found in the Flash boot sector, are protected in the Slave-side Flash when the FLASHPRT2 is asserted (**low**). To unprotect the Flash boot sector, reset unlock bit FLUNLCK2 at BCSR6.1 and then write **high** in the FLASHPRT2 bit. This allows for further erase/write operations in the boot sector.	0	R,W
2	FRM_RST	***E1/T1 Framer Reset***. The FALC56 device is reset when the FRM_RST is asserted (**low**). The HRESETh signal of the MSC8101 will assert the FRM_RST signal.	1	R/W
3	CODEC_EN	***CODEC Enable.*** The Mitel MT92303 CODEC chip is selected for the serial control bus and is programmable when the CODEC_EN bit is asserted (**low**). The CODEC device is disabled for programming purposes when negated **(high)**.	1	R,W
4	SIGNALS0	***Signal LED Slave 0***. A dedicated Green LED is illuminated when SIGNALS0 is active (**low**). The LED is unlit when in its inactive (default) state **(high)**. During the Reset Configuration sequence the LED indicates the state of Slave HRESETs assertion. The user may utilize the LED for s/w Slave signalling purposes.	1	R,W
5	SIGNALS1	***Signal LED Slave 1***. A dedicated Red LED is illuminated when SIGNALS1 is active (**low**). The LED is unlit when in its inactive (default) state **(high)**. During the Reset Configuration sequence the LED indicates the state of Slave SRESETs assertion. The user may utilize the LED for s/w Slave signalling purposes.	1	R,W
6	SIGNALH0	***Signal LED Host 0.*** A dedicated Green LED is illuminated when SIGNALH0 is active (**low**). The LED is unlit when in its inactive (default) state **(high)**. During the Reset Configuration sequence the LED indicates the state of Host HRESETh assertion. The user may utilize the LED for s/w Host signalling purposes.	1	R,W
7	SIGNALH1	***Signal LED Host 1***.A dedicated Red LED is illuminated when SIGNALH1 is active (**low**). The LED is unlit when in its inactive (default) state **(high)**. During the Reset Configuration sequence the LED indicates the state of Host SRESETh assertion. The user may utilize the LED for s/w Host signalling purposes.	1	R,W
8-31	-	Not Implemented.	-	-

4.12.2 BCSR1 - Board Control / Status Register 1

On the ADS, the BCSR1 acts as a control register and is accessed from the BCSR base address as a **byte** at **offset 0x4**. The BCSR1, which may be read or written at any time, receives its defaults upon main Power-On-Reset or HRESET. The BCSR1 fields are described below in *Table 4-10 "BCSR1 Description"*:

Table 4-10 BCSR1 Description

BIT	MNEMONIC	Function	DEF	ATT.
0	RECONF	***Start Slave Re-configuration.*** Bit RECONF is associated with the Slave PRSTs signal and, when set **(low)**, enables performance of the Slave's secondary Power-on-Reset configuration. When negated **(high)** the bit has no influence on the state of the board.	1	W

Table 4-10 BCSR1 Description

BIT	MNEMONIC	Function	DEF	ATT.
1	HRST1	***Hard Reset to Slave1.*** The HRST1 signal is asserted to external off-board Slave1 when bit HRST1 is set **(low)**. When negated **(high)** the bit has no influence on the state of the HRST1 signal. Reading the bit results in the sampling of external off-board Slave1 and, as such, provides an indication of the Slave processor's state.	1	R,W
2	HRST2	***Hard Reset to Slave2.*** The HRST2 signal is asserted to external off-board Slave2 when bit HRST2 is set **(low)**. When negated **(high)** the bit has no influence on the state of the HRST2 signal. Reading the bit results in the sampling of external off-board Slave2 and, as such, provides an indication of the Slave processor's state.	1	R,W
3	ATM_RST	***ATM Peripheral Reset.*** Upon activation **(low)** the ATM port transceiver enters into a reset state. The same applies to the ATM_RST signal when the HRESETh signal of the MSC8101 is asserted.	1	R,W
4	HRST3	***Hard Reset to Slave3.*** The HRST3 signal is asserted to external off-board Slave3 when bit HRST3 is set **(low)**. When negated **(high)** the bit has no influence on the state of the HRST3 signal. Reading the bit results in the sampling of external off-board Slave3 and, as such, provides an indication of the Slave processor's state.	1	R,W
5	FETH_RST	***Fast Ethernet Peripheral Reset.*** Upon activation **(low),** the PHY LSI 80225 enters into a reset state and the MII port control bits revert to their default values. The same applies to the FETH_RST signal when the HRESETh signal of the MSC8101 is asserted.	1	R,W
6	RS232EN_1	***RS232 Transceiver Host-side Enable***. Upon activation **(low),** the RS232 Transceiver, using the SCC1 port of the Host MSC8101, is enabled. When negated (**high**), the RS232 Transceiver enters standby mode.	1	R,W
7	RS232EN_2	***UART Transceiver Slave-side Enable***. Upon activation **(low),** the MSC8102 UART port transceiver is enabled. When negated (**high**), the RS232 Transceiver enters standby mode and the UART port pins become available for off-board use (via the J5 expansion connectors).	1	R,W
8-31	-	Not Implemented.	-	-

4.12.3 BCSR2 - Board Control / Status Register 2

On the ADS, the BCSR2 serves as both a control register and a MSC8102 Slave configuration setting. It is accessed from the BCSR base address as a **byte** at **offset 0x8** and, it should be noted, may be read or written at any time. Depending upon the Slave Configuration DIP Switch SW4/3 (SYS/DSI) setting, the BCSR2 receives its defaults upon main Power-On-Reset or HRESETh. The BCSR2 fields are described below in *Table 4-11 "BCSR2 Register Description"*:

Table 4-11 BCSR2 Register Description

BIT	MNEMONIC	Function	DEFAULT SYS	DEFAULT DSI	ATT.
0	RSTCNF	***Reset Configuration Mode.*** During the Slave Power-on-Reset configuration sequence the RSTCNF signal drives the logical level of the bit's value. The user may, at any time, change the value of bit RSTCNF.	0		R,W
1	CNFG	***Configuration Source.*** During the Slave Power-on-Reset configuration sequence the CNFG signal drives the logical level of the bit's value. After the sequence the signal enters the Hi-Z state. The user may, at any time, change the value of bit CNFG.	0	1	R,W
2	SWTE	***Software Watchdog Timer Enable.*** During the Slave Power-on-Reset configuration sequence the SWTE signal drives the logical level of the bit's value. After the sequence the signal enters the Hi-Z state. After completing the configuration process negation occurs (**low**) and the s/w watchdog timer is disabled. If asserted (**high**) then the s/w watchdog timer is enabled.	1	0	R,W
3	DSI64	***DSI /System 64/32 -bit.*** The DSI64 signal indicates DIP Switch SW7/3 and is permanently set at the time of main Power-on-Reset. After the sequence the signal enters the Hi-Z state. When negated (**low**) the DSI bus configures to 32-bit and the System bus to 64-bit. If asserted (**high**) the DSI bus configures to 64-bit and the System bus to 32-bit.	-		R
4	DSISYNC	***DSI Synchronous Mode.*** During the Slave Power-on-Reset configuration sequence the DSISYNC signal drives the logical level of the bit's value. After the sequence the signal enters the Hi-Z state. When negated (**low**) the DSI bus configures to an asynchronous mode or, if asserted (**high),** to a synchronous mode. The latter mode is not supported in MSC8101 Host.	0		R,W
5	HRST	***Hard Reset to Slave.*** The $\overline{\text{HRESETs}}$ signal is asserted to the on-board MSC8102 Slave when bit HRESETs is set **(low)**. When negated **(high)** the bit has no influence on the state of the HRESETs signal. Reading the bit results in the sampling of the MSC8102 Slave and, as such, provides an indication of the Slave processor's state.	1		R,W
6	SRST	***Soft Reset to Slave.*** The $\overline{\text{HRESETs}}$ signal is asserted to the on-board MSC8102 Slave when bit HRESETs is set **(low)**. When negated **(high)** the bit has no influence on the state of the HRESETs signal. Reading the bit results in the sampling of the MSC8102 Slave and, as such, provides an indication of the Slave processor's state.	1		R,W
7	FRMtoTSI	***E1/T1 Framer to TSI device***. The TDM channels of the FALC56 device are connected to a TSI device when the FRM to TSI is asserted (**low**). When the FRMtoTSI is negated **(high)** the TDM channels of the FALC56 device are tied directly to a TDM3 port of the MSC8102. Both muxing instances occur via a bus switch.	1		R,W
8-31	-	Not Implemented.	-	-	-

4.12.4 BCSR3 - Board Control / Status Register 3

On the ADS, the BCSR3 serves as both a control register and a Slave (MSC8102) configuration setting. It is accessed from the BCSR base address as a **byte** at **offset 0xc** and, it should be noted, may be read or written at any time. Depending upon the Slave Configuration DIP Switch SW4

setting, the BCSR3 receives its defaults upon main Power-On-Reset or HRESET. The BCSR3 fields are described below in *Table 4-12 "ADS BCSR3 Register Description"*:

.

Table 4-12 ADS BCSR3 Register Description

BIT	*MNEMONIC*	*Function*	*DEF AULT*		*ATT.*
			SYS	*DSI*	
0-1	CLKMD[1:2]	***Clock Mode Setting Bits 1-2 for Slave.*** During the Slave Power-on-Reset configuration sequence the CLKMD signals drive the logical level of the bit's value. After the sequence the signals enter the Hi-Z state. The user may, at any time, change the value of bits CLKMD[1:2].	From DIP Switch SW4/1-2		R,W
2	SEE0	***Slave Emulation Enable 0.*** Bit SEE0 controls the Slave debug request. When bit SEE0 is asserted **(low)** then PLD logic generates a short positive pulse for the Slave EE0 input. Consequently MSC8102 enters debug mode despite the DIP Switch SW4/4 setting. Toggling the DIP Switch SW4/4 (DBG) setting achieves the same results as those described above. Reading bit SEE0 results in the sampling of the MSC8102 EE0 signal state.	Slave EE0 signal		R,W
3-4	Reserved	Not Implemented.	'11'		R
5-7	BTMD[0:2]	***Boot Mode Bits 0-2.*** During the Slave Power-on-Reset configuration sequence the BTMD signals drive the logical level of the bit's value. After the sequence the signals enter the Hi-Z state. The user may, at any time, change the value of bits BTMD[0:2]	'000'	'001'	R,W
8-31	-	Not Implemented.	-	-	-

Table 4-13 Summary Slave Configuration Modes

DSI/SYS DIP Switch	*MSC8102 Config. Inputs*				*Slave Configuration Description*
	BM[0:2]	SWTE	RSTCNF	CNFGS	
On	'001'	0	0	1	Configuration & Boot performed through DSI bus.
Off	'000'	1	0	0	Configuration & Boot performed through System bus when MSC8102 is a Boot Master.

4.12.5 BCSR4 - Board Status Register - 4

BCSR4 is a status register accessed from the BCSR base address as a **byte** at **offset 0x10**. BCSR4 is a **Read-Only** register that may be read at any time. The BCSR4 fields are described

below in *Table 4-14 "BCSR4 Description"*:

Table 4-14 BCSR4 Description

BIT	*MNEMONIC*	*Function*	*DEF SET*	*ATT.*
0-1	SEE[0:1]	***Slave Emulation Enable Bits 0-1.*** Bits SEE[0:1] illustrate the state of the Slave's EE0 and EE1 lines.	-	R
2-4	SWOPT[0:2]	***Software Option 0-2***. Bits SWOPT[0:2] illustrate the state of dedicated DIP Switch SW5/1-3. This DIP Switch provides the option for manually changing a program's flow.	SW5/1-3 DIP Switch	R
5-7	Reserved	Not Implemented.	'111'	R
8-31	-	Not Implemented.	-	-

4.12.6 BCSR5 - Board Identification Register - 5

BCSR5 is a **Read-Only** register accessed from the BCSR base address as a **byte** at **offset 0x14**. The BCSR5 fields are described below in *Table 4-15 "BCSR5 Description"*:

Table 4-15 BCSR5 Description

BIT	*MNEMONIC*	*Function*	*ATT.*
0-1	BCONF[0:1]	***Board Configuration Type***. Field BCONF[0:1] represents the ADS configuration type. See *Table 4-16 "ADS Configuration Encoding"* for ADS configuration encoding.	R
2-4	BREVN[0:2]	***Board Revision Number 0-2***. Field BREVN[0:2] represents the ADS revision code. See *Table 4-17 "ADS Revision Encoding"* for revised ADS encoding.	R
5-7	BCSRREV[0:2]	***BCSR Revision Number 0-2***. Field BCSRREV[0:2] represents the revised BCSR code. See *Table 4-18 "BCSR Revision Encoding"* for revised BCSR encoding.	R
8-31	-	Not Implemented.	-

Table 4-16 ADS Configuration Encoding

Configuration Code[0:1]	*ADS Configuration*
0	ADS - the complete ADS includes both the MSC8101and MSC8102 processors
1	ADSs - the single ADS includes only the MSC8102 processor
2-3	Reserved

Table 4-17 ADS Revision Encoding

Revision Number [0:2]	*ADS Revision*
0	PROTO

Table 4-17 ADS Revision Encoding

Revision Number [0:2]	*ADS Revision*
1	PILOT
2	A
3 - 7	Reserved

Table 4-18 BCSR Revision Encoding

Revision Number [0:2]	*BCSR Revision*
0-7	1.x - 8.x

4.12.7 BCSR6 - Board Miscellaneous Register - 6

BCSR6 is a service register accessed from the BCSR base address as a **byte** at **offset 0x16**. The BCSR6 fields are described below in *Table 4-19 "BCSR6 Description"*.

Table 4-19 BCSR6 Description

BIT	*MNEMONIC*	*Function*	*DEF*	*ATT.*
0	FLUNLCK1	***Flash 1 Protection Unlock.*** The default for hardware write protection bit FLUNLCK1 is negation **(high)** and consequently bit BCSR0.0 FLASHPRT1 is locked. In order to unlock bit BCSR0.0 FLASHPRT1 then bit FLUNLCK1 must be asserted **(low)**.	1	R,W
1	FLUNLCK2	***Flash 2 Protection Unlock.*** The default for hardware write protection bit FLUNLCK2 is negation **(high)** and consequently bit BCSR0.1 FLASHPRT2 is locked. In order to unlock bit BCSR0.1 FLASHPRT2 then bit FLUNLCK2 must be asserted **(low)**.	1	R,W
2-6	Reserved	Not Implemented.	1	-
7	Reserved	Not Implemented.	0	-
8-31	-	Not Implemented.	-	-

Section 5 Support Info

5.1 Memory Map

5.1.1 Host 60-x Bus Mapping

The MSC8101 Memory Controller governs all access to the MSC8101 memory slaves. Consequently the memory map may be reprogrammed according to user needs. After performing Hard Reset, the debug host may initialize the memory controller via the P14 connector at the JTAG/OnCE port as this allows additional access to bus addressable peripherals. The SDRAM and FLASH memory respond to all types of memory access - program/data and Direct Memory Access (DMA).

Table 5-1 Host MSC8101 Memory Map

ADDESS RANGE	*Memory Type*	*Device Name*	*Volume in Byte*	*Port Size in Bit*
00000000 - 0007FFFF	Internal SRAM[a]	MSC8101 Internal Space		64
00080000 - 00EFFDFF	Empty Space			
00EFFE00 - 00EFFEFF	EOnCE Registers[a]			
00EFFF00 - 00EFFFFF	Empty Space			
00F00000 - 00F0FFFF	DSP Peripherals (Qbus Bank0)			
00F10000 - 00F7FFFF	Empty Space			
00F80000 - 00F807FF	Boot ROM (Qbus Bank1)			
00F80800 - 01EFFFF	Empty Space			
01F00000 - 01F0FFFF	DSP Peripherals (CS11)			
01F10000 - 01FFFFFF	Empty Space			
02000000 - 0207FFFF	Internal SRAM (CS10)			
02080000 - 144FFFFF	Empty Space			
14500000 - 14507FFF 14500000 14500004 14500008 1450000C 14500010 14500014 14500018	BCSR(0:5): BCSR0 BCSR1 BCSR2 BCSR3 BCSR4 BCSR5 BCSR6	ALTERA EPM3256 resides on 60-x Bus	32K[b]	8
14508000 - 145FFFFF	Empty Space		-	-
14600000 - 14607FFF	ATM SONET Framer Proc. Control	PM5384	32K[c]	8
14608000 - 146FFFFF	Empty Space		-	-
14700000[d] - 1483FFFF	MSC8101 60-x Bus Memory and CPM[e]	MSC8101 Internal Space	128K	32
14840000 - 1FFFFFFF	Empty Space		-	-
20000000 - 20FFFFFF	SDRAM	MT48LC2M32B2 x 2	16M	64
21000000 - 23FFFFFF	Empty Space		-	-

Table 5-1 Host MSC8101 Memory Map

ADDESS RANGE	*Memory Type*	*Device Name*	*Volume in Byte*	*Port Size in Bit*
24000000 - 241FFFFF	Slave0 (off-board) DSI Bus	MSC8102 ID 0	2M	32/64[f]
• • •	• • •	• • •		
25E00000 - 25FFFFFF	Slave15 (on-board) DSI Bus	MSC8102 ID 15	2M	32/64[f]
26000000 - 261FFFFF	Broadcast Access over DSI Bus	All MSC8102	2M	32/64[f]
26200000 - FFBFFFFF	Empty Space		-	-
FFC00000 - FFFFFFFF	Flash	Am29LV320	4M	16

a. The internal SDRAM is mapped to fixed addresses in the SC140 core. Refer to the MSC8101 spec for a complete description of the SC140 Core internal memory map. [2].
b. The 32KB device appears repeatedly in port-size (byte) x depth multiples. For example, BCSR0 appears at memory locations 14700000, 14700010, 14700020..., while BCSR1 features at 14700004, 14700014, 14700024... and so on.
c. The internal space of the ATM SONET Framer control port is 256 bytes, however, the minimum block size controllable by a CS region is 32KB. The same logic applies to other peripherals.
d. After the Hard Reset configuration sequence is finished then MSC8101 internal registers are automatically placed in the hF0000000 - hF000FFFF address area. Following this the Host debugger tool initializes a re-configured memory space as shown in *Table 5-1 "Host MSC8101 Memory Map"*.
e. The MSC8101 spec comprehensively describes the MSC8101 Internal Memory Map.
f. The DSI port size is dependant upon the MSC8102 Power-on-Reset configuration pin.

The memory map defined in *Table 5-1 "Host MSC8101 Memory Map"* is only a recommendation for the user can choose to work with alternative memory mapping. It should be noted that the described mode is supported by Metrowerks' CodeWarrior debug tool.

5.1.2 Slave System Bus Mapping

The MSC8102 Memory Controller governs all access to the MSC8101 memory slaves. Consequently the memory map may be reprogrammed according to user needs. After performing Hard Reset, the debug host may initialize the memory controller via connectors P14 or P15 at the JTAG/OnCE port for this allows additional access to bus addressable peripherals. SDRAM and FLASH-memory respond to all types of memory access - program / data and DMA.

.

Table 5-2 Slave MSC8102 Memory Map

ADDRESS RANGE	*Memory Type*	*Device Name*	*Config*	*Volume in Byte*	*Port Size in Bit*
00000000 - 00037FFF	L1 Memory on Internal Bus[a]	MSC8102 Internal Space	Any	224K	64
00038000 - 00EFFDFF	Empty Space				
00EFFE00 - 00EFFFFF	EOnCE				
00F00000 - 00F0FFFF	DSP Peripherals (Qbus Bank0)				
00F10000 - 00FFFFFF	Empty Space				
01000000 - 01076FFF	L2 Memory (MQbus)			480 KB	
01077000 - 01077FFF	Boot ROM (MQbus)				
01078000 - 017FFFFF	Empty Space				
01800000 - 01FFFFFF	SQbus Internal Space				
02000000 - 02076FFF	L2 Memory (System bus)			480 KB	
02077000 - 02077FFF	Boot ROM (System bus)				
02080000 - 020B7FFF	L1MEM0 (System bus)			224 KB x4	
020C0000 - 020F7FFF	L1MEM1 (System bus)				
02100000 - 02137FFF	L1MEM2 (System bus)				
02140000 - 02177FFF	L1MEM3 (System bus)				
02178000 -0217FFFF	Empty Space				
02180000 - 021BFFFF	CS9 - (IP address space)				
021E0000 - 021FFFFF	CS10 - (EFCOP,FDIR, FDOR)				
02200000 -145FFFFF	Empty Space				
14600000 - 14607FFF	Time-Slot-Interchanger (TSI)	PEF24471		32K[b]	8
14608000 - 1460FFFF	FALC56 E1/T1 Framer	PEB2256		32K[c]	8
14610000 - 146FFFFF	Empty Space		-	-	-
14700000[d] - 14713FFF	MSC8102 System I/F	MSC8102 Internal Space	-	128K	32
14820000 - 1FFFFFFF	Empty Space		-	-	-
20000000 - 20FFFFFF OR 20000000 - 208FFFFF	SDRAM	MT48LC2M32B 2 x 2 MT48LC2M32B 2 x 1	64-bit SysBus 32-bit SysBus	16M 8M	64 32
22000000 - FFBFFFFF	Empty Space			-	-
FFC00000 - FFFFFFFF	Flash	Am29LV320		4M	8

a. L1 Memory is mapped to fixed addresses in the SC140 core. See the MSC8102 spec for a complete description of the SC140 Core internal memory map *[1].*

b. The TSI device's internal space is 32 bytes, however, the minimum block size controllable by a CS region is 32KB.

c. The E1/T1 FALC56 Framer device's internal space is 256 bytes, however, the minimum block size controllable by a CS region is 32KB.

d. After the Hard Reset configuration sequence is finished then MSC8101 internal registers are automatically placed in the hF0000000 - hF000FFFF address area. Following this the Host debugger tool initializes a re-configured memory space as shown in *Table 5-2 "Slave MSC8102 Memory Map"*

5.2 Host Memory Controller Registers' Programming

The MSC8101 Memory Controller in the MSC8102ADS is initialized for an 100/66 MHz bus operation. For example, programming of the registers is based on a 100/66 MHz timing calculation.

Warning

Initializations noted in *Table 5-3 "Host's Memory Controller Initialization for 100(66) MHz" below* **are based on ADS board design.**

Table 5-3 Host's Memory Controller Initialization for 100(66)[a] MHz

Reg.	Device Type	Bus	Init Value [hex]	Description
BR0	Am29LV320 by AMD	Buffered 60-x	FFC01001	Base at FFC0_0000, 16-bit port size, no parity, GPCM.
OR0			FFC00874 (FFC00854)	4MB block size, CS early negate, 14(10) w.s., Timing relax.
BR1	BCSR0-6 Implemented in Altera EPM3256	Buffered 60-x	14501801	Base at 14500_000, 32-bit port size, no parity, GPCM.
OR1			FFFF8820 (FFFF8810)	32 KB block size, all types access, CSNT=1, 2 w.s. (32 KB block size, all types access, CSNT=1, 1 w.s.)
BR2	SDRAM 64-bit Supported	Non-buffered 60-x	20000041	Base at 2000_0000, 64-bit port size, no parity, SDRAM machine 1.
OR2	SDRAM MT48LC2M32B2T6-8x2 by Micron		FF003080	16MB block size, 4 banks per device, row starts at A8, 11 row lines, internal bank interleaving allowed.
BR3	MSC8102 DSI Port broadcast CS	Non-buffered 60-x	26001801	Base at 2800_0000, 32-bit port size, no parity, GPCM.
			26000001	Base at 2800_0000, 64-bit port size, no parity, GPCM.
OR3			FFE00844 (FFE00884)	2MB block size, CSNT, four/eight wait states, TRLX.
BR4	MSC8102 DSI Port	Non-buffered 60-x	24001881	Slave's based at 2400_0000 (on-Board Slave based at 2600_0000), 32-bit port size, no parity, UPMA.
			24000081	Slave's based at 2400_0000 (on-Board Slave based at 2600_0000), 64-bit port size, no parity, UPMA.
OR4			FE000100 (FE000100)	32MB block size, non-burst.
BR5	PM5384 - ATM UNI	Buffered 60-x	146008A1	Base at 1460_0000, 8-bit port size, UPMB.
OR5			FFFF8100	32KB block size, non-burst.
BR6	User's peripheral	Buffered PPC	-	-
OR6			-	-
BR10	DSPRAM	Local PPC	020000C1	Base at 0020_0000, 64-bit port size, no parity, UPMC.
OR10			FFF80000	512KB block size.
BR11	DSP Peripherals	Local PPC	01F00021	Base at 01F0_0000, 64-bit port size, no parity, GPCM on local PPC bus.
OR11			FFFF0000	64KB block size

Table 5-3 Host's Memory Controller Initialization for 100(66)[a] MHz

Reg.	Device Type	Bus	Init Value [hex]	Description
PSDMR	SDRAM 64-bit	Non-buff-ered PPC	C26B36A7 (C2692452)	Page interleaving, refresh enabled, normal operation, address muxing mode SDAM=2, A(15-17) on BNK-SEL(0:2), A8 on PSDA10, 8(4) clocks refresh recovery, 3(2) clocks precharge to activate delay, 3(2) clocks acti-vate to read/write delay, 4 beat burst length, 2(1) clock last data out to precharge, 2(1) clock write recovery time, internal address muxing, normal timing, buffered (non-buffered), 3(2) clocks CAS latency.
PSRT	SDRAM Supported	All PPC Bus Config.	13	Generates refresh every 14 µsec instead of the outside limit of every 15.6 µsec. Thus the refresh redundancy is 6.6 msec. The full SDRAM refresh cycle needs 64 msec. For example, application s/w may withhold the 60x bus for up to approx. 6.6 msec in a 57.3 msec period without jeopardizing the contents of the 60x bus SDRAM.
MPTPR	SDRAM Supported		2800(1300)	Divide Bus clock by 40D (20D)

a. Table values marked with parentheses are indicative of the lower 66 MHz frequency bus.

-

Table 5-4 MAMR Programming (CS4:DSI)

Step	Register Name	Value to write	Description
Single Write	MAMR	0x10048898	The noted value allows an array write operation to control the write routine; UPMWAIT enabled; read/write loop performed twice.
	MDR	0x0FFFCC00	CS active & GPL2 are active
	MDR	0x0CFFCC00	BS active, WAEN enable
	MDR	0x00FFDD00	BS active, WAEN disable, begin loop
	MDR	0x0FFFCC04	BS active, end loop
	MDR	0x0FFFCF00	
	MDR	0x0FFFCC01	End access
Single Read	MAMR	0x10C48880	The noted value allows an array write operation to control the read routine; UPMWAIT enabled; read/write loop performed twice.
	MDR	0x0FFFCC00	Only CS active
	MDR	0x0FFECC00	BS active, WAEN enable
	MDR	0x0FFCDD00	BS active, WAEN disable, begin loop
	MDR	0x0FFCCC04	BS active, end loop
	MDR	0x0FFFCF00	CS negated, end access
	MDR	0x0FFFCC01	CS negated, end access

Table 5-4 MAMR Programming (CS4:DSI)

Step	Register Name	Value to write	Description
Exception	MAMR	0x10C488BC	The noted value allows an array write operation to control the exception routine; UPMWAIT enabled; read/write loop performed twice.
	MDR	0xFFFFCC05	Access termination
Run	MAMR	0x00C48880	Normal operation

Table 5-5 MBMR Programming (CS5:ATM)

Set	Register Name	Value to write	Description
Single Write	MBMR	0x10011018	The noted value allows an array write operation to control the write routine; read/write loop performed four times.
	MDR	0x0FFFFC00	CS active is active
	MDR	0x00FFFC80	BS active, begin loop
	MDR	0x00FFFC80	BS active, end loop
	MDR	0xFFFFFC00	CS negated & BS negated
	MDR	0xFFFFFF05	End access
Single Read	MBMR	0x10011000	The noted value allows an array write operation to control the read routine; read/write loop performed seven times.
	MDR	0x0FFFFC00	CS active
	MDR	0x0FFCFC80	GPL2 active, begin loop
	MDR	0x00FCFC80	GPL2 active, end loop
	MDR	0x0FFCFC04	GPL2 active, PSDVAL asserted
	MDR	0x00FFFD00	
	MDR	0xFFFFFF01	End access
Exception	MBMR	0x1001103C	The noted value allows an array write operation to control the exception routine.
	MDR	0xFFFFCC05	
Run	MBMR	0x00011000	Normal operation

5.3 Slave Memory Controller Registers' Programming

The MSC8102 Memory Controller in the MSC8102ADS is initialized for an 100/66 MHz bus operation. For example, programming of the registers is based on a 100/66 MHz timing calculation.

Warning

Initializations noted in *Table 5-6 "Slave's Memory Controller Initialization for 100(66) MHz" below* **are based on ADS board design.**

Table 5-6 Slave's Memory Controller Initialization for 100(66)[a] MHz

Reg.	Device Type	Bus	Init Value [hex]	Description
BR0	Am29LV320 by AMD	Buffered System Bus	FFC00801	Base at FFC0_0000, 8-bit port size, no parity, GPCM.
OR0			FFC00874 (FFC00854)	4MB block size, CS early negate, 14(10) w.s., Timing relax.
BR1	NC	-	-	-
OR1			-	-
BR2	SDRAM 64-bit Supported	Non-buffered System Bus	20000041	Base at 2000_0000, 64-bit port size, no parity, SDRAM machine 1.
OR2	SDRAM MT48LC2M32B2T6-8x2 by Micron		FF0030a0	16MB block size, 4 banks per device, row starts at A8, 11 row lines, internal bank interleaving allowed.
BR2	SDRAM 32-bit Supported	Non-buffered System 32-bit configuration	20001841	Base at 2000_0000, 32-bit port size, no parity, SDRAM machine 1.
OR2	MT48LC2M32B2T6-8 by Micron		FF8032a0	8MB block size, 4 banks per device, row starts at A9, 11 row lines, internal bank interleaving allowed.
BR3	TSI	Buffered System Bus	14600881	Base at 1460_0000, 8-bit port size, no parity, UPMA.
OR3			FFFF8100	32 KB block size, non-burst.
BR4	E1/T1 FALC	Buffered System Bus	14680881	Base at 1468_0000, 8-bit port size, no parity, UPMA.
OR4			FFFF8100	32 KB block size, non-burst.
CS5-CS7	Not used	-	-	User define
BR9	IP Bus	Internal System Bus	02181821	Base at 218_0000, 32-bit port size, no parity, GPCM local bus.
OR9			FFFC0008	256KB block size, non-burst.
BR10	EFCOP	Internal System Bus	021E0021	Base at 21E0_0000, 64-bit port size, no parity, GPCM local bus
OR10			FFFF0000	64 KB block size, non-burst
BR11	L1's & L2	Internal System Bus	020000C1	Base at 2000_0000, 64-bit port size, no parity, UPMC
OR11			FFE00000	2M block size, non-burst.

Table 5-6 Slave's Memory Controller Initialization for 100(66)[a] MHz

Reg.	Device Type	Bus	Init Value [hex]	Description
PSDMR	SDRAM 64-bit	Non-buffered System Bus	C26B36A7 (C2692452)	Page interleaving, refresh enabled, normal operation, address muxing mode SDAM=2, A(15-17) on BNK-SEL(0:2), A8 on PSDA10, 8(4) clocks refresh recovery, 3(2) clocks precharge to activate delay, 3(2) clocks activate to read/write delay, 4 beat burst length, 2(1) clock last data out to precharge, 2(1) clock write recovery time, Internal address muxing, normal timing, 3(2) clocks CAS latency.
	SDRAM 32-bit	Non-buffered System Bus	C28737A7 (C2432552)	Page interleaving, refresh enabled, normal operation, address muxing mode 1, A(13-15) on BNKSEL(0:2), A9 on PSDA10, 8(4) clocks refresh recovery, 3(2) clocks precharge to activate delay, 3(2) clocks activate to read/write delay, 8 beat burst length, 2(1) clock last data out to precharge, 2(1) clock write recovery time, Internal address muxing, normal timing, 3(2) clocks CAS latency.
PSRT	SDRAM Supported	All System Bus Config.	13	Generates refresh every 14 µsec instead of the outside limit of every 15.6 µsec. Thus the refresh redundancy is 6.6 msec. The full SDRAM refresh cycle needs 64 msec. For example, application s/w may withhold the System bus for up to approx. 6.6 msec in a 57.3 msec period without jeopardizing the contents of the System bus SDRAM.
MPTPR	SDRAM Supported		2800(1300)	Divide Bus clock by 40D (20D).

a. Table values marked with parentheses are indicative of the lower 66MHz frequency bus.

Table 5-7 MAMR Programming (CS3:TSI & CS4:E1/T1 FALC)

Step	Register Name	Value to write [hex]	Description
Single Write	MAMR	10015418	The noted value allows an array write operation to control the write routine; read/write loop performed five times.
	MDR	FFFFFD00	Address setup
	MDR	0FFFFC00	CS active
	MDR	0FF33C80	GPL1(WR TSI) & GPL3(WR FALC) low, start loop
	MDR	0FF33C80	GPL1(WR TSI) & GPL3(WR FALC) low, stop loop
	MDR	0FFFFC00	GPL1(WR TSI) & GPL3(WR FALC) high
	MDR	3FFFFC05	PSDVAL asserted, end access

Table 5-7 MAMR Programming (CS3:TSI & CS4:E1/T1 FALC)

Step	Register Name	Value to write [hex]	Description
Single Read	MAMR	10015400	The noted value allows an array write operation to control the read routine; read/write loop performed five times.
	MDR	FFFFFD00	Address setup
	MDR	0F0CFC80	CS active, GPL0(RD TSI) & GPL2(RD FALC) low, stop loop
	MDR	0F0CFC04	CS active, GPL0(RD TSI) & GPL2(RD FALC) low, PSDVAL asserted
	MDR	FFFFFC00	CS negated, GPL0(RD TSI) & GPL2(RD FALC) high
	MDR	FFFFFD00	Double idle cycle
	MDR	FFFFFC01	End access
Exception	MAMR	1001543C	The noted value allows an array write operation to control the read routine.
	MDR	FFFFCC05	Access termination
Run	MAMR	00015400	Normal operation

Table 5-8 MCMR Programming (CS9:L1s & L2 Memory)

Step	Register Name	Value to write [hex]	Description
Single Write	MCMR	90051258	The noted value allows an array write operation to control the write routine; read/write loop performed four times
	MDR	00000040	Exception enable
	MDR	00000045	Access termination
Burst Write	MCMR	90051260	The noted value allows an array write operation to control the burst write routine; read/write loop performed four times.
	MDR	00000C48	Increment address
	MDR	00000C4C	Increment address with PSDVAL assertion - first beat
	MDR	00000C4C	Increment address with PSDVAL assertion- second beat
	MDR	00000044	PSDVAL assertion - third beat
	MDR	00000045	PSDVAL assertion - fourth beat with access termination
Single Read	MCMR	90051240	The noted value allows an array write operation to control the read routine; read/write loop performed four times.
	MDR	00030040	GPL2 is high, exception enable
	MDR	00030045	GPL2 is high, access termination

Step	Register Name	Value to write [hex]	Description
Burst Read	MCMR	90051248	The noted value allows an array write operation to control the burst read routine; read/write loop performed four times.
	MDR	00030C48	GPL2 is high, increment address
	MDR	00030C4C	GPL2 is high, increment address with PSDVAL assertion - first beat
	MDR	00030C4C	GPL2 is high, increment address with PSDVAL assertion -second beat
	MDR	00030044	GPL2 is high with PSDVAL assertion -third beat
	MDR	00030045	GPL2 is high, PSDVAL assertion - fourth beat with access termination
Exception	MCMR	9005127C	The noted value allows an array write operation to control the exception routine.
	MDR	FF000001	Access termination
Run	MCMR	80011240	Normal operation

5.4 Power

5.4.1 Power Supplies

There are three power buses:

1) 3.3V for the on-board Logic and I/O of two processors.
2) 1.5V for the Host MSC8101 Core and PLL.
3 1.5V for the Slave MSC8102 Core and PLL.

Both processor PLL's will obtain filtering voltage from their Core power supply.

The main 3.3V supply is a high-performance DC-to-DC converter that provides up to a 4A current for on and off -board loads. In addition are the two regular 1.5V linear voltage regulators that produce quiet voltage for the processors. A suppressor Diode protects the board from the application of reverse voltage.

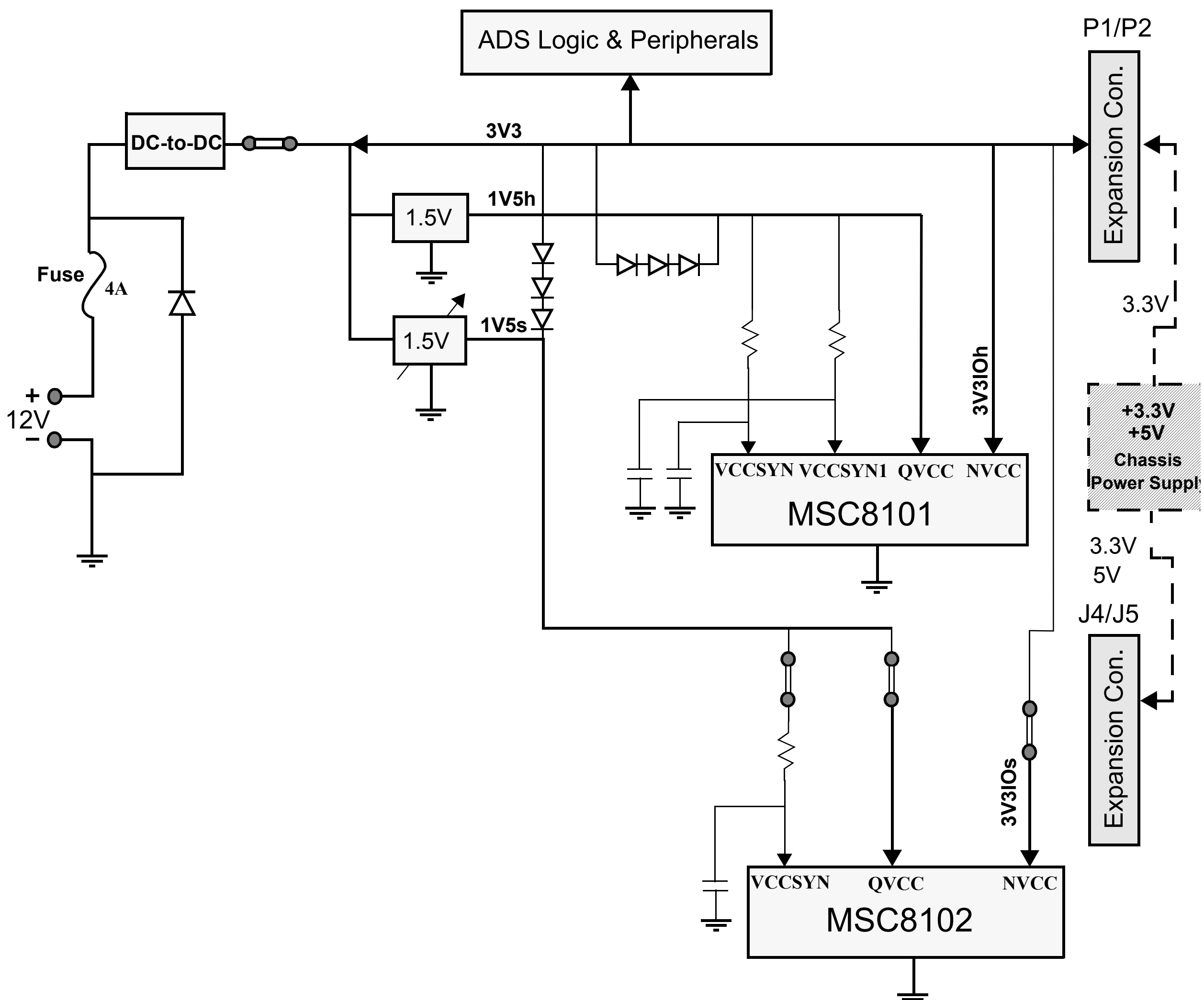


Figure 5-1 ADS Power Scheme

To support off-board application development, a 3.3V power bus is connected to expansion con-

nectors J1/J2. In this way external logic, mounted on a prototype board, may be powered directly from the main ADS. It is strongly recommended that off-board cases with high current consumption.

5.5 Interconnect Signals

The MSC8102ADS interconnects with external devices via the following set of connectors:

1) P1,P5 - 3.5mm Stereo Phone Jack
2) P2 - RF SMB Socket
3) P3, P4, P7, P9, P11, P12, P16, P18 to P22 - 11 Logic Analyzer MICTOR Connectors
4) P6 - RJ45 for E1/T1 port
5) P8 - D-type9 90^0 Female RS232 Port
6) P10 - Three pins header for Slave’s UART Port
7) P13 - PLD Altera’s In System Programming (ISP)
8) P14 - Host JTAG/ONCE
9) P15 - Slave JTAG/ONCE
10) P17 - Two pins header for EE1 MSC8102 debug request chain
11) P20 - RJ45 100/10 - Base-T Ethernet port
12) P23 - Power Supply
13) J1-J5 - Expansion Connectors

5.5.1 P1,P5 - Stereo Phone Jack Connectors

These are stereo 5-pin headphone connector with pinout as shown in *Table 5-9 "P1,P5 - Stereo Phone Connectors Interconnect Signals" below*

Table 5-9 P1,P5 - Stereo Phone Connectors Interconnect Signals

Pin No.	Signal Name	Description
1	COMMON	Analog Ground. Connect to AGND1 plane.
2	LEFT	Left channel
3	RIGHT	Right channel
10	SPEAKER LEFT	Not connected
11	SPEAKER RIGHT	Not connected

5.5.2 P2 - SMB Connector

RF Subminiature Coaxial Connector P2 is intended for an external clock source for MSC8102 when jumper JP4/2-3 is close.

5.5.3 Logic Analyzer Connectors

There are P3, P4, P7, P9, P11, P12, P16, P18 to P22 - 38 pin, SMT, high density, matched impedance connector made by AMP used for Logic Analyzer measurement. They contain all MSC8101 signals unbuffered. The pinout of these connectors is shown in MSC8102ADS Schematics.

5.5.4 P6 - RJ45 E1/T1 Line Connector

The E1/T1 connector is Twisted-Pair compatible connector. It is implemented with a 90^{o}, 8-pin, RJ45 connector, signals of which are described in *Table 5-10 "P6 - E1/T1 Line Connector Interconnect Signals" below*

Table 5-10 P6 - E1/T1 Line Connector Interconnect Signals

Pin No.	Signal Name	Description
1	RX1+	Twisted-Pair Receive Data positive **input** from the MSC8102ADS.
2	RX1-	Twisted-Pair Transmit Data positive **input** from the MSC8102ADS.
3	GND	Digital Ground plane.
4	TX1+	Twisted-Pair Transmit Data positive **output** from the MSC8102ADS.
5	TX1-	Twisted-Pair Transmit Data negative **output** from the MSC8102ADS.
6	GND	Digital Ground plane.
7	N.C.	Not Connected.
8		

5.5.5 P10 - Slave UART Port Connector

The RS232 port connector - P10 is 9 pin, 90^{o}, female D-Type shielded connector, signals of which are presented in *Table 5-11 "P10 Interconnect Signals"*

Table 5-11 P10 Interconnect Signals[a]

Pin No.	Signal Name	Description
1,6	DTR	Data Terminal Ready **output** from the MSC8102ADS shorted to pin 1.
2	TXD	Transmit Data **output** from the MSC8102ADS.
3	RXD	Receive Data **input** to the MSC8102ADS.
4	DSR	Data Set Ready **input** to the MSC8102ADS.
5	GND	Ground signal of the MSC8102ADS.
7	CTS	Clear To Send **input** to the MSC8102ADS.
8	RTS	Ready To Send **output** from the MSC8102ADS.
9	N.C.	Not connected

a. Refer to *Figure 4-12 "Slave UART Serial Port Connector" on page 61*.

5.5.6 P13 - Altera's In System Programming (ISP)

This is a 10 pin generic 0.100" pitch header connector, providing In System Programming capability for Altera CPLD devices made programmable logic on board. The pinout of P13 is shown in *Table 5-12 "P13 - ISP Connector - Interconnect Signals" below*:

Table 5-12 P13 - ISP Connector - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
1	TCK	I	ISP Test port Clock. This clock shifts in / out data to / from the programmable logic JTAG chain.
2	GND	P	Digital GND. Main GND plane.
3	TDO	O	ISP Transmit Data Output. This the prog. logic's JTAG serial data output driven by Falling edge of TCK.
4	VCC	P	Connect to 3.3V power supply bus for feeding an external programmer logic.
5	TMS	I	ISP Test Mode Select. This signal qualified with TCK, changes the state of the prog. logic JTAG machine.
6	N.C.	-	Not Connected.
7	N.C.	-	Not Connected.
8	N.C.	-	Not Connected.
9	TDI	I	ISP Transmit Data In. This is the prog. logic's JTAG serial data input..
10	GND	P	Digital GND. Main GND plane.

5.5.7 P14 - Host Debug OnCE (SYS) Connector

P14 is a Motorola standard JTAG/ONCE connector for the DSP. It is a 14 pin 90^{o} two row header connector with key. Host debug may access through connector P14 to all processors joned by JTAG chain. The pinout of P14 is shown in *Table 5-13 "P14 - Main ONCE Connector - Inter-*

connect Signals" below:

Table 5-13 P14 - Main ONCE Connector - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
1	TDIh	I	Transmit Data In. This is the JTAG serial data input of the MSC8101, sampled on the rising edge of TCK.
2	GND	P	Digital GND. Main GND plane.
3	TDOhc	O	Transmit Data Output. This the DSP JTAG serial data output driven by Falling edge of TCK.
4	GND	P	Digital GND. Main GND plane.
5	TCKhc	I	Test port Clock. This clock shifts in / out data to / from the JTAG logic. Data is driven on the falling edge of TCK and is sampled both internally and externally on it's rising edge.
6	GND	P	Digital GND. Main GND plane.
7	N.C.	-	Not Connected.
8	KEY	-	No pin in connector. Serve for correct plug insertion.
9	HRESEThb	I/O,P.U.	When asserted by an external H/W, generates Hard-Reset sequence for the MSC8101. During that sequence, asserted by the MSC8101 for 512 system clocks. Pulled Up on the ADS using a 1KΩ resistor. When driven by an external tool, **MUST be driven with an Open Drain gate. Failure to do so might result in permanent damage to the MSC8101 and / or to ADS logic.**
10	TMSh	I	Test Mode Select. This signal qualified with TCK in a same manner as TDI, changes the state of the JTAG machines. This line is pulled up internally by the MSC8101.
11	VDD	P	Connect to 3.3V power supply bus via protection resistor. May be used for Command Convertor power.
12	N.C.	-	Not Connected.
13			
14	TRSThb	I	Test port Reset. When this signal is active (Low), it resets the JTAG logic. This line is pull-down on the ADS with a 2.2KΩ resistor, to provide continuous reset of the JTAG logic, when connector is unplugged.

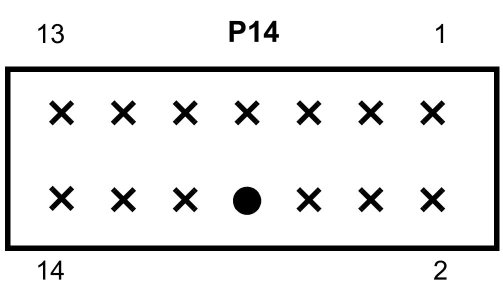


Figure 5-2 P14 connector front view

5.5.8 P15 - Slave Debug OnCE (SLV) Connector

P15 is a Motorola standard JTAG/ONCE connector for the DSP. It is a 14 pin straight two row header connector with key. Host debug may access through connector P15 to MSC8102 when separate JTAG chain mode is chosen by DIP SW7/1,2 switch. The pinout of P15 is shown in *Table 5-14 "P15 - Slave ONCE Connector - Interconnect Signals" below*:

Table 5-14 P15 - Slave ONCE Connector - Interconnect Signals

Pin No.	Signal Name	Attribute	Description
1	TDIsc	I	Transmit Data In. This is the JTAG serial data input of the MSC8102, sampled on the rising edge of TCK.
2	GND	P	Digital GND. Main GND plane.
3	TDOsc	O	Transmit Data Output. This the MSC8102's JTAG serial data output driven by Falling edge of TCK.
4	GND	P	Digital GND. Main GND plane.
5	TCKsc	I	Test port Clock. This clock shifts in / out data to / from the JTAG logic. Data is driven on the falling edge of TCK and is sampled both internally and externally on it's rising edge.
6	GND	P	Digital GND. Main GND plane.
7	N.C.	-	Not Connected.
8	KEY	-	No pin in connector. Serve for correct plug insertion.
9	HRESETsb	I/O,P.U.	When asserted by an external H/W, generates Hard-Reset sequence for the MSC8102. During that sequence, asserted by the MSC8102 for 512 system clocks. Pulled Up on the ADS using a 1KΩ resistor. When driven by an external tool, **MUST be driven with an Open Drain gate. Failure to do so might result in permanent damage to the MSC8102 and / or to ADS logic.**
10	TMSsc	I	Test Mode Select. This signal qualified with TCK in a same manner as TDI, changes the state of the JTAG machines. This line is pulled up internally by the MSC8102.
11	VDD	P	Connect to 3.3V power supply bus via protection resistor. May be used for Command Convertor power.
12	N.C.	-	Not Connected.
13			
14	TRSTscb	I	Test port Reset. When this signal is active (Low), it resets the MSC8102 JTAG logic. This line is pull-down on the ADS with a 2.2KΩ resistor, to provide continuous reset of the JTAG logic, when connector is unplugged.

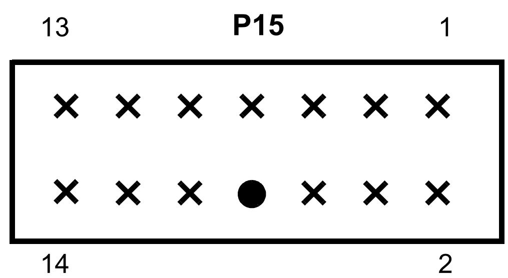


Figure 5-3 P15 connector top view

5.5.9 P17 - EE1 Connector

EE1 two pins header on the ADS front side which provide MSC8102 debug request connectivity on the another ADS boards. The pinout of P17 is shown in *Table 5-15 "P17 - EE1 Chain Connector" below* :

Table 5-15 P17 - EE1 Chain Connector

Pin No.	Signal Name	Attribute	Description
1	EE1in	I	Debug Request to the on-board MSC8102
2	EEout	O	Debug Request to MSC8102 mounted on another board (ADSs)

5.5.10 P20 - Ethernet Port Connector

The Ethernet connector on the MSC8102ADS - P20, is a Twisted-Pair (10-Base-T) compatible connector. It is implemented with a 90^{o}, 8-pin, RJ45 connector, signals of which are described in *Table 5-16 "P20 - Ethernet Port Interconnect Signals" below*

Table 5-16 P20 - Ethernet Port Interconnect Signals

Pin No.	Signal Name	Description
1	TPTX(GRAY)	Twisted-Pair Transmit Data positive **output** from the MSC8102ADS.
2	TPTX~(BROWN)	Twisted-Pair Transmit Data negative **output** from the MSC8102ADS.
3	TPRX(YELLOW)	Twisted-Pair Receive Data positive **input** to the MSC8102ADS.
4	(RED,GREEN)	Bob Smith terminated on the MSC8102ADS.
5		
6	TPRX~(BLACK)	Twisted-Pair Receive Data negative **input** to the MSC8102ADS.
7	(BLUE,ORANGE)	Bob Smith terminated on the MSC8102ADS.
8		

5.5.11 P23 Power Connector

P23 is 2mm Power Jack RAPC722 provide connection to external power supply +12VDC@1.8A.

5.5.12 J1 to J5 cPCI Connector

These connectors carry MSC8101 60x bus signals and MSC8102 peripheral signals out for off-board connection. :

Table 5-17 J1 - 60x Bus System Expansion

Pin No.	Signal Name	Attribute	Description
A1	-	N.C.	Not connected
A2	XTCK	O	JTAG Clock for off-board ADS placed at a backplane
A3	-	N.C.	Not connected
A4	XCS6	O	Chip Select 6 of the MSC8101
A5	XA18	O	60x Buffered Address Line 18
A6	IRQ2hb	I,P.U.	Interrupt 2 to the MSC8101. Pulled up on the ADS with a 10 KΩ resistor.
A7	XD30	I/O	60x Buffered Data Line 30
A8	XD26	I/O	60x Buffered Data Line 26
A9	XBS3	O	Buffered Byte Select 3 Strobe
A10	XD21	I/O	60x Buffered Data Line 21
A11	XD18	I/O	60x Buffered Data Line 18
A12-A14	Not populated	-	-
A15, A17, A19, A21, A23	3V3	P	+3.3V Power. External power supply can feed the ADS via back-plane.
A16	XHBCSb	O	Broadcast Chip Select for off-board ADS is associated with MSC8101 CS3.
A17	XA12	O	60x Buffered Address Line 12
A20	XD12	I/O	60x Buffered Data Line 12
A22	XD7	I/O	60x Buffered Data Line 7
A24	XD1	I/O	60x Buffered Data Line 1
A25	N.C.	-	Not Connected
B1-B4	N.C.	-	Not Connected
B5	XA17	O	60x Buffered Address Line 17
B6, B8, B10, B16, B18, B20, B22	GND	P	Digital Ground. Connected to main GND plane of the ADS.
B7	XD29	I/O	60x Buffered Data Line 29
B11	N.C.	-	Not Connected
B12-B14	Not populated	-	-

Table 5-17 J1 - 60x Bus System Expansion

Pin No.	Signal Name	Attribute	Description
B15	XHCSb	O	Chip Select for off-board ADS is associated with MSC8101 CS4
B17	XA14	O	60x Buffered Address Line 14
B19	XD15	I/O	60x Buffered Data Line 15
B21	XD9	I/O	60x Buffered Data Line 9
B23	XD4	I/O	60x Buffered Data Line 4
B25	XA9	O	60x Buffered Address Line 9
C1	TRSThb	O	Reset to JTAG port for off-board ADS
C2	XTMS	O	TMS to JTAG port for off-board ADS
C3	N.C.	-	Not Connected
C4, C6, C8, C10, C16, C18, C20, C22, C24	GND	P	Digital Ground. Connected to main GND plane of the ADS.
C5	PRSTsb	O, O.D.	Power-On-Reset signal for Slaves (MSC8102)
C7	XD28	I/O	60x Buffered Data Line 28
C9	XD23	I/O	60x Buffered Data Line 23
C11	XD16	I/O	60x Buffered Data Line 16
C12-C14	Not populated	-	-
C15	XGPL2	O	Expansion General Purpose Line 2. This is buffered strobe which assist MSC8101 UPM control over memory device if necessary. May be used as OE for GPCM.
C17	XA13	O	60x Buffered Address Line 13
C19	XD14	I/O	60x Buffered Data Line 8
C21	XD8	I/O	60x Buffered Data Line 3
C23	XD3	I/O	60x Buffered Data Line 28
C25	XA7	O	60x Buffered Address Line 7
D1	N.C.	-	Not Connected
D2	TDOo	O	TDO signal is driven by off-board ADS.
D3	N.C.	-	Not Connected
D4	XA19	O	60x Buffered Address Line 19
D5, D7, D9, D11, D17, D19	GND	P	Digital Ground. Connected to main GND plane of the ADS.
D6	CLKX	O	60x Buffered Bus Clock
D8	XD25	I/O	60x Buffered Data Line 25
D10	XD20	I/O	60x Buffered Data Line 20
D12-D14	Not populated	-	-
D15	N.C.	-	Not Connected

Table 5-17 J1 - 60x Bus System Expansion

Pin No.	Signal Name	Attribute	Description
D16	GPL4(UPMWAIThb)	I/O, O.D.	Expansion General Purpose Line 4. This signal is configured as UPMWAIThb Open Drain for Slaves I/F and pulled up on the ADS with 10 KΩ resistor
D18	XA15	O	60x Buffered Address Line 15
D20	XD11	I/O	60x Buffered Data Line 11
D22	XD6	I/O	60x Buffered Data Line 6
D24	XD0	I/O	60x Buffered Data Line 0
D25	3V3	P	+3.3V Power. External power supply can feed the ADS via back-plane.
E1	N.C.	-	Not Connected
E2	TDIi	I	TDI signal is driven by the ADS to off-board.
E3,E4	N.C.	-	Not Connected
E5	HRST1b	I/O, O.D.	Hard Reset signal for off-board ADS located at first peripheral slot. This signal is pulled up on the ADS with 10 KΩ resistor
E6	XD31	I/O	60x Buffered Data Line 31
E7	XD27	I/O	60x Buffered Data Line 27
E8	XD24	I/O	60x Buffered Data Line 24
E9	XD22	I/O	60x Buffered Data Line 22
E10	XD19	I/O	60x Buffered Data Line 19
E11	XBS2	O	Buffered Byte Select 2 Strobe
E12-E14	Not populated	-	-
E15	N.C.	-	Not Connected
E16	XA11	O	60x Buffered Address Line 11
E17	XA10	O	60x Buffered Address Line 10
E18	XBS1	O	Buffered Byte Select 1 Strobe
E19	XD13	I/O	60x Buffered Data Line 13
E20	XD10	I/O	60x Buffered Data Line 10
E21	XBS0	O	Buffered Byte Select 0 Strobe
E22	XD5	I/O	60x Buffered Data Line 5
E23	XD2	I/O	60x Buffered Data Line 2
E24	XA8	O	60x Buffered Address Line 8
E25	N.C.	-	Not Connected
F1-F25	Shield	-	Connected to chassis.

Table 5-18 J2 - 60x Bus System Expansion

Pin No.	Signal Name	Attribute	Description
A1-A3	-	N.C.	Not connected
A4	3V3	P	+3.3V Power. External power supply can feed the ADS via back-plane.
A5	XBS5	O	Buffered Byte Select 5 Strobe
A6	XD63	I/O	60x Buffered Data Line 63
A7	XD59	I/O	60x Buffered Data Line 59
A8	XD56	I/O	60x Buffered Data Line 56
A9	XD52	I/O	60x Buffered Data Line 52
A10	XD49	I/O	60x Buffered Data Line 49
A11	XD45	I/O	60x Buffered Data Line 45
A12	XD42	I/O	60x Buffered Data Line 42
A13	XD38	I/O	60x Buffered Data Line 38
A14	XD35	I/O	60x Buffered Data Line 35
A15	XA21	O	60x Buffered Address Line 21
A16	XA24	O	60x Buffered Address Line 24
A17	XA25	O	60x Buffered Address Line 25
A18	XA29	O	60x Buffered Address Line 29
A19	GND	P	Digital Ground. Connected to main GND plane of the ADS.
A20-A22	-	N.C.	Not connected
B1, B3, B5, B7, B9, B11, B13, B15, B17, B19, B20, B21	GND	P	Digital Ground. Connected to main GND plane of the ADS.
B2	N.C.	-	Not Connected
B4	XA20	O	60x Buffered Address Line 20
B6	XD62	I/O	60x Buffered Data Line 62
B8	XD55	I/O	60x Buffered Data Line 55
B10	XD48	I/O	60x Buffered Data Line 48
B12	XD41	I/O	60x Buffered Data Line 41
B14	XD34	I/O	60x Buffered Data Line 34
B16	XA23	O	60x Buffered Address Line 23
B18	XA28	O	60x Buffered Address Line 28
B22	GA3	I, P.U.	Line 3 of Geographic Addressing sets up by jumper on the back-plane. This signal is pulled up on the ADS with 10 KΩ resistor
C1	IRQ3hb	I,P.U.	Interrupt 3 to the MSC8101. Pulled up on the ADS with a 10 KΩ resistor.

Table 5-18 J2 - 60x Bus System Expansion

Pin No.	Signal Name	Attribute	Description
C2	SYSENb	O	This pin is grounded on the System Slot of the backplane that allow to enable 60x bus strobes transceiver. Pulled up on the ADS with a 10 KΩ resistor.
C3	HRESETsb	I/O, O.D.	Hard Reset signal for on-board Slave (MSC8102). This signal is pulled up on the ADS with 1 KΩ resistor
C4	XBS7	O	Buffered Byte Select 7 Strobe
C5, C7, C9, C11, C13	GND	P	Digital Ground. Connected to main GND plane of the ADS.
C6	XD61	I/O	60x Buffered Data Line 61
C8	XD54	I/O	60x Buffered Data Line 54
C10	XD47	I/O	60x Buffered Data Line 47
C12	XD40	I/O	60x Buffered Data Line 40
C14	XD33	I/O	60x Buffered Data Line 33
C15, C16	N.C.	-	Not Connected
C17	HRESEThb	I/O, O.D.	Hard Reset signal for on-board Host (MSC8101) provides Power-On-Reset for off-board ADS. This signal is pulled up on the ADS with 1 KΩ resistor
C18	XA27	O	60x Buffered Address Line 27
C19	XGPL0	O	Expansion General Purpose Line 0. This is buffered strobe which assist MSC8101 UPM control over memory device if necessary. May be used on a rear board.
C20	XGPL1	O	Expansion General Purpose Line 1. This is buffered strobe which assist MSC8101 UPM control over memory device if necessary. May be used on a rear board.
C21	XGPL3	O	Expansion General Purpose Line 3. This is buffered strobe which assist MSC8101 UPM control over memory device if necessary. May be used on a rear board.
C22	GA2	I, P.U.	Line 2 of Geographic Addressing sets up by jumper on the back-plane. This signal is pulled up on the ADS with 10 KΩ resistor
D1	HRST2b	I/O, O.D.	Hard Reset signal for off-board ADS located at second peripheral slot. This signal is pulled up on the ADS with 10 KΩ resistor
D2	HRST3b	I/O, O.D.	Hard Reset signal for off-board ADS located at third peripheral slot. This signal is pulled up on the ADS with 10 KΩ resistor
D3	N.C.	-	Not Connected
D4, D6, D8, D10, D12, D14, D16, D18, D20	GND	P	Digital Ground. Connected to main GND plane of the ADS.
D5	XBS4	O	Buffered Byte Select 4 Strobe
D7	XD58	I/O	60x Buffered Data Line 58
D9	XD51	I/O	60x Buffered Data Line 51
D11	XD44	I/O	60x Buffered Data Line 44

Table 5-18 J2 - 60x Bus System Expansion

Pin No.	Signal Name	Attribute	Description
D13	XD37	I/O	60x Buffered Data Line 37
D15, D17	N.C.	-	Not Connected
D19	XPSDVALb	O	60x Buffered Data Valid Strobe. May be used on a rear board
D21	N.C.	-	Not Connected
D22	GA1	I, P.U.	Line 1 of Geographic Addressing sets up by jumper on the back-plane. This signal is pulled up on the ADS with 10 KΩ resistor
E1	IRQ4hb	I,P.U.	Interrupt 4 to the MSC8101. Pulled up on the ADS with a 10 KΩ resistor.
E2, E3	N.C.	-	Not Connected
E4	XBS6	O	Buffered Byte Select 6 Strobe
E5	XA16	O	60x Buffered Address Line 16
E6	XD60	I/O	60x Buffered Data Line 60
E7	XD57	I/O	60x Buffered Data Line 57
E8	XD53	I/O	60x Buffered Data Line 53
E9	XD50	I/O	60x Buffered Data Line 50
E10	XD46	I/O	60x Buffered Data Line 46
E11	XD43	I/O	60x Buffered Data Line 43
E12	XD39	I/O	60x Buffered Data Line 39
E13	XD36	I/O	60x Buffered Data Line 36
E14	XD32	I/O	60x Buffered Data Line 32
E15	N.C.	-	Not Connected
E16	XA22	O	60x Buffered Address Line 22
E17	N.C.	-	Not Connected
E18	XA26	O	60x Buffered Address Line 26
E19	BXBCTL0	O	Buffer Control Strobe 0. May be use on a rear board.
E20	BAh31	O	60x Buffered Address Line 31. May be use on a rear board.
E21	BAh30	O	60x Buffered Address Line 30. May be use on a rear board.
E22	GA0	I, P.U.	Line 0 of Geographic Addressing sets up by jumper on the back-plane. This signal is pulled up on the ADS with 10 KΩ resistor
F1-F22	Shield	-	Connected to chassis

Table 5-19 J4 - H.110 Bus

Pin No.	Signal Name	Attribute	Description
A1	HTD0	I/O	Bus Data Line 0
A2	HTD4	I/O	Bus Data Line 4

Table 5-19 J4 - H.110 Bus

Pin No.	Signal Name	Attribute	Description
A3	HTD8	I/O	Bus Data Line 8
A4	HTD11	I/O	Bus Data Line 11
A5	HTD13	I/O	Bus Data Line 13
A6	HTD16	I/O	Bus Data Line 16
A7	HTD19	I/O	Bus Data Line 19
A8	HTD21	I/O	Bus Data Line 21
A9	HTD24	I/O	Bus Data Line 24
A10	HTD27	I/O	Bus Data Line 27
A11	HTD29	I/O	Bus Data Line 29
A12-A25	Not in use	-	-
B1	3V3	P	+3.3V Power. External power supply can feed the ADS via back-plane.
B2	HTD5	I/O	Bus Data Line 5
B3	HTD9	I/O	Bus Data Line 9
B4	5V0	P	+5.0V Power. External power supply can feed the ADS via back-plane.
B5	HTD14	I/O	Bus Data Line 14
B6	HTD17	I/O	Bus Data Line 17
B7	5V0	P	+5.0V Power. External power supply can feed the ADS via back-plane.
B8	HTD22	I/O	Bus Data Line 22
B9	HTD25	I/O	Bus Data Line 25
B10	3V3	P	+3.3V Power. External power supply can feed the ADS via back-plane.
B11	HTD30	I/O	Bus Data Line 30
B12-B22	Not in use	-	-
B23	CT_RESETb	O	Reset to H.110 device on the ADS.
B24	N.C.	-	Not Connected
B25	HSGA3	I, P.U.	Line 3 of Shelf Enumeration sets up by jumper on the backplane. This signal is pulled up on the ADS with 10 KΩ resistor
C1	HTD1	I/O	Bus Data Line 1
C2	HTD6	I/O	Bus Data Line 6
C3	HTD10	I/O	Bus Data Line 10
C4	HTD12	I/O	Bus Data Line 12
C5	HTD15	I/O	Bus Data Line 15
C6	HTD18	I/O	Bus Data Line 18

Table 5-19 J4 - H.110 Bus

Pin No.	Signal Name	Attribute	Description
C7	HTD20	I/O	Bus Data Line 20
C8	HTD23	I/O	Bus Data Line 23
C9	HTD26	I/O	Bus Data Line 26
C10	HTD28	I/O	Bus Data Line 28
C11	HTD31	I/O	Bus Data Line 31
C12-C22	Not in use	-	-
C23	CT_ENb	I, P.U.	This signal indicates that the ADS is fully seated into backplane. Pull-up value is 2.4KΩ resistor
C24	N.C.	-	Not Connected
C25	HSGA2	I, P.U.	Line 2 of Shelf Enumeration sets up by jumper on the backplane. This signal is pulled up on the ADS with 10 KΩ resistor
D1	HTD2	I/O	Bus Data Line 2
D2	HTD7	I/O	Bus Data Line 7
D3, D6, D7, D9	GND	P	Digital Ground. Connected to main GND plane of the ADS.
D4, D5	3V3	P	+3.3V Power. External power supply can feed the ADS via back-plane.
D8, D10	5V0	P	+5.0V Power. External power supply can feed the ADS via back-plane.
D10	XD20	I/O	60x Buffered Data Line 20
D11-D24	Not in use	-	-
D25	HSGA1	I, P.U.	Line 1 of Shelf Enumeration sets up by jumper on the backplane. This signal is pulled up on the ADS with 10 KΩ resistor
E1	HTD1	I/O	Bus Data Line 1
E2	GND	P	Digital Ground. Connected to main GND plane of the ADS.
E3	HSCLK_D	I/O	Skewed 8 MHz SCbus compatibility Data Clock
E4	HSCLK	I/O	8 MHz SCbus compatibility Data Clock
E5	HTNETREF_2	I/O	Secondary Telecom Network Timing Reference
E6	HTNETREF_1	I/O	Primary Telecom Network Timing Reference
E7	HT_C8_B	I/O	8 MHz redundant Data Clock
E8	HT_C8_A	I/O	8 MHz Data Clock
E9	HFR_COMP	I/O	8 KHz SCbus compatibility Frame Clock
E10	HT_FRAME_B	I/O	Redundant 8 KHz Frame Clock
E11	HT_FRAME_A	I/O	8 KHz Frame Clock
E12-E24	Not in use	-	-
E25	HSGA0	I, P.U.	Line 0 of Shelf Enumeration sets up by jumper on the backplane. This signal is pulled up on the ADS with 10 KΩ resistor

Table 5-19 J4 - H.110 Bus

Pin No.	Signal Name	Attribute	Description
F1-F15	GND	P	Digital Ground. Connected to main GND plane of the ADS.
F12-F20	Not populated	-	-
F21-F25	Shield	-	Connected to chassis.

Table 5-20 J5 - MSC8102 Signal Expansion Connector

Pin No.	Signal Name	Attribute	Description
A1	DSTo	O	Serial Data from CODEC
A2	N.C.	-	Not Connected
A3	L4TXD	O	MSC8101 TDM Port 4 Transmit Data
A4	GND	P	Digital Ground. Connected to main GND plane of the ADS.
A5	L4RXD	I	MSC8101 TDM Port 4 Receive Data
A6	L3TXD	O	MSC8101 TDM Port 3 Transmit Data
A7	L3RXD	I	MSC8101 TDM Port 3 Receive Data
A8	L2TXD	O	MSC8101 TDM Port 2 Transmit Data
A9	L2RXD	I	MSC8101 TDM Port 2 Receive Data
A10	L1TXD	O	MSC8101 TDM Port 1 Transmit Data
A11	L1RXD	I	MSC8101 TDM Port 1 Receive Data
A12	TD_A3	O	MSC8102 TDM Port 3 Transmit Data A channel
A13	RD_A3	I	MSC8102 TDM Port 3 Receive Data A channel
A14	TD_A2	O	MSC8102 TDM Port 2 Transmit Data A channel
A15	RD_A2	I	MSC8102 TDM Port 2 Receive Data A channel
A16	TD_A1	O	MSC8102 TDM Port 1 Transmit Data A channel
A17	RD_A1	I	MSC8102 TDM Port 1 Receive Data A channel
A18	TD_A0	O	MSC8102 TDM Port 0 Transmit Data A channel
A19	3V3	P	+3.3V Power. External power supply can feed the ADS via back-plane.
A20	RD_A0	I	MSC8102 TDM Port 0 Receive Data A channel
A21	TESTs	I,O	High active Test Signal for MSC8102.
A22	TIMER0	I/O	MSC8102 Timer 0.
B1	N.C.	-	Not Connected
B2, B4, B6, B8, B10, B12, B14, B16, B18, B20, B22	GND	P	Digital Ground. Connected to main GND plane of the ADS.
B3, B5	N.C.	-	Not Connected

Table 5-20 J5 - MSC8102 Signal Expansion Connector

Pin No.	Signal Name	Attribute	Description
B7	L4CLK	I	MSC8101 TDM Port 4 Data Clock
B9	L2CLK	I	MSC8101 TDM Port 2 Data Clock
B11	TDMCLK3	I	MSC8102 TDM Port 3 Data Clock
B13	TDMCLK2	I	MSC8102 TDM Port 2 Data Clock
B15	TDMCLK1	I	MSC8102 TDM Port 1 Data Clock
B17	TDMCLK0	I	MSC8102 TDM Port 0 Data Clock
B19	TIMER3	I/O	MSC8102 Timer 3
B21	TIMER1	I/O	MSC8102 Timer 1
C1	DSTi	I	Serial Data from CODEC
C2-C4	N.C.	-	Not Connected
C5	L3CLK	I	MSC8101 TDM Port 3 Data Clock
C6, C8, C10, C12 C14, C16, C18	3V3	P	+3.3V Power. External power supply can feed the ADS via back-plane.
C7	L1CLK	I	MSC8101 TDM Port 1 Data Clock
C9	GPCLK1	O	Programmable General Purpose Clock1 from the TSI part (U16)
C11	GPCLK0	O	Programmable General Purpose Clock0 from the TSI part (U16)
C13	TD_B3	O	MSC8102 TDM Port 3 Transmit Data B channel
C15	TD_B2	O	MSC8102 TDM Port 2 Transmit Data B channel
C17	TD_B1	O	MSC8102 TDM Port 1 Transmit Data B channel
C19	TD_B0	O	MSC8102 TDM Port 0 Transmit Data B channel
C20	CCLK	I	CODEC Data Clock for Serial Microport
C21	GND	P	Digital Ground. Connected to main GND plane of the ADS.
C22	TIMER_CLK2	I/O	MSC8102 Timer 2
D1	F0	I	CODEC Frame Alignment
D2	N.C.	-	Not Connected
D3, D5, D7, D9, D11, D17, D19	GND	P	Digital Ground. Connected to main GND plane of the ADS.
D4, D6	N.C.	-	Not Connected
D8	L3SYNC	I	MSC8101 TDM Port 3 Frame Sync
D10	L1SYNC	I	MSC8101 TDM Port 1 Frame Sync
D12	TDMSYN3	I	MSC8102 TDM Port 3 Frame Sync
D14	TDMSYN2	I	MSC8102 TDM Port 2 Frame Sync
D16	TDMSYN1	I	MSC8102 TDM Port 1 Frame Sync
D18	TDMSYN0	I	MSC8102 TDM Port 0 Frame Sync
D20	CDATA	I/O	CODEC Data I/O

Table 5-20 J5 - MSC8102 Signal Expansion Connector

Pin No.	Signal Name	Attribute	Description
D21	EE0s	I/O	MSC8102 Debug Reguest Pin (EE0)
D22	UARTRX	I	MSC8102 UART Recieve Pin
E1	N.C.	-	Not Connected
E2	TDIi	I	TDI signal is driven by the ADS to off-board.
E3,E4	N.C.	-	Not Connected
E5	HRST1b	I/O, O.D.	Hard Reset signal for off-board ADS located at first peripheral slot. This signal is pulled up on the ADS with 10 KΩ resistor
E6	XD31	I/O	60x Buffered Data Line 31
E7	XD27	I/O	60x Buffered Data Line 27
E8, E10, E12, E15, E17, E19	GND	P	Digital Ground. Connected to main GND plane of the ADS.
E9	XD22	I/O	60x Buffered Data Line 22
E10	XD19	I/O	60x Buffered Data Line 19
E11	XBS2	O	Buffered Byte Select 2 Strobe
E14	3V3	P	+3.3V Power. External power supply can feed the ADS via back-plane.
E15	N.C.	-	Not Connected
E16	XA11	O	60x Buffered Address Line 11
E17	XA10	O	60x Buffered Address Line 10
E18	XBS1	O	Buffered Byte Select 1 Strobe
E19	XD13	I/O	60x Buffered Data Line 13
E20	XD10	I/O	60x Buffered Data Line 10
E21	XBS0	O	Buffered Byte Select 0 Strobe
E22	XD5	I/O	60x Buffered Data Line 5
E23	XD2	I/O	60x Buffered Data Line 2
E24	XA8	O	60x Buffered Address Line 8
E25	N.C.	-	Not Connected
F1-F22	Shield	-	Connected to chassis.

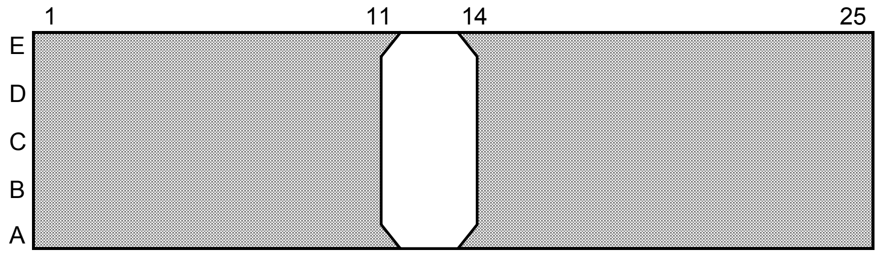


Figure 5-4 cPCI J1,J4 connectors view

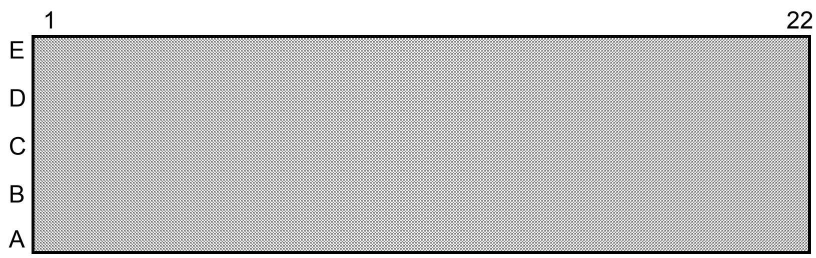


Figure 5-5 cPCI J2,J5 connectors view

5.6 Program Information

The MSC8102ADS has one programmable logic device - Altera CPLD, serving control and stasus function on the ADS. It implemented an U18 EPM3256ATC144-7. The design is done in Verilog HDL program format and is listed below:

```
// renoir header_start
//
// Module BCSR_L1.BCSR_main.Main
//
// Created:
//          by - msil_lab.UNKNOWN (PC287)
//          at - 11:34:53 05/09/01
//
// Generated by Mentor Graphics' Renoir(TM) 2000.3 (Build 2)
//
// renoir header_end

`resetall
`timescale 1ns/10ps


module BCSR_main (
          clk,extclk,Data,reset,A7,A8,A9,A10,A27,A28,A29,
          /*nPSDVAL,*/nWE,nW_R,nCS0,nBCSR_CS,nATMCS,nFCSh,nHCS1,nHBCS,
          DSItoSYS,nSYS64,nFCFG,MODCK1s,MODCK2s,SWOPT,nSTBUFEN,
      nRS232EN_1,nRS232EN_2,nFETH_RST,nATM_RST,nFRM_RST,FRMtoTSI,nCODEC_EN,
nBOOTPh,nBOOTPs,nDBUFXEN,nDBUFBEN, GA, nPRSTs,
          HEE0_In,HEE0_Out,HEE1_In,HEE1_Out,
          SEE0_In,SEE0_Out,SEE1_In,EE1_misc_In, EE1_misc_Out,n32to64En,
      SIGH_LED,SIGS_LED,SEE1_LED,nLED_EN,
      Aborth_In, HReseth_In, SReseth_In, Aborts_In, HResets_In, SResets_In,
      MODCK1h,MODCK2h,MODCK3h,MODCK4h,MODCK5h,MODCK6h,MODCKh_Out,
      nHRESETh,nSRESETh,nHRESETs,nSRESETs,nHRST,nHRST_In,nNMIh,nNMIs,
BM_Out,CNFGS_Out,DSI64_Out,DSISYNC_Out,SWTE_Out,MODCK1s_Out,MODCK2s_Out,
RSTCFG_Out,TEST_EN,TEST_SIG
  );

//*** General Definition ***//
`define   ASSERTED      0
`define   NEGATED       1
`define  ACTIVE_LOW 0
`define   ACTIVE_HIGH    1
`define   PRESSED       0
`define   RELEASED      1
`define  WRITE     1
`define  READ     0
`define   From_BCSR      1
`define   From_FLASH     0
parameter BCSR_ver      = 3'b010; // Current version of code is 2
parameter divpr         = 12;
parameter divsee0       = 2;
parameter div2st        = 5;//3; // 4 // to apply delay equals 'delay = extclk * 2**10' or 50usec@20Mhz
parameter div1st        = 13;//2;//16 // to apply delay equals 'delay = extclk * 2**20' or 50msec@20Mhz
parameter zero          = 1'b0;
parameter divd          = div2st;
```

```
parameter divc          = div1st;

//*** Inputs ***//
input clk,              // From Host clock buffer
     extclk,     // Clock from external clock oscillator
  reset;      // Main Power-on-Reset
input A27,A28,A29,      // 60-x bus addresses lines
     /*nPSDVAL*/nWE,nW_R,      //    and controls
  nCS0,nBCSR_CS,nATMCS, // Chip selects
     DSItoSYS,          // DIP-switch selectes Slave boot source
  nSYS64,            // DIP-switch selectes Slave data bus distribution
  nFCFG,  // DIP-switch selectes Host boot source (BCSR or Flash)
  MODCK1s,MODCK2s,  // DIP-switch select MODCKl for the Slave
     MODCK1h,MODCK2h,MODCK3h,
  MODCK4h,MODCK5h,MODCK6h; // DIP-switch select MODCKl for the Host
input       nHCS1,nHBCS;  // Chip Selects for Slaves
input       A7,A8,A9,A10; // Addresses together with nHCS1,2 & nHBCS for select Slaves on/off- board
input [0:3] GA;          // Geographic Address of System Board setting by on-CPCI backplane jumpers,
                         // default value equals 0xf
input       Aborth_In, Aborts_In,    // Pushbuttons of NMI for Host & Slave
           HReseth_In, HResets_In,  // Pushbuttons of HReset for Host & Slave
SReseth_In, SResets_In;  // Pushbuttons of Sreset for Host & Slave
input       HEE0_In,HEE1_In; // Inputs from DIP-switch for Host EE0,1 control
input       SEE0_In,SEE1_In; // Inputs from DIP-switch for Slave EE0,1 control
input       EE1_misc_In; // Debug acknowledge comming from another ADS
input [0:2] SWOPT;        // Software options applied from DIP-switch
input [1:3] nHRST_In;              // Three HRESETs from external boards
//*** Bidirectional ***//
inout [0:7] Data;   // Eight bit of buffered 60-x bus
inout       nHRESETh,nHRESETs, // HRESET for Host & Slave
           nSRESETh,nSRESETs; // SRESET for Host & Slave
inout       nPRSTs;          // Wire connected to PORESET of Slave
inout       HEE1_Out;         // EE1 for Host
//*** Outputs ***//
output      nNMIh,nNMIs;          // IRQ0 for Host & Slave
output      nFCSh,               // Host Side Flash chip enable
            nRS232EN_1,nRS232EN_2, // Enable for RS232 transmitters
 nFETH_RST,nATM_RST,// Reset for ATM framer and Ethernet Phy
 nFRM_RST,    // E1/T1 Farmer Reset
 FRMtoTSI,            // Switch FALC56 channels to TSI or to TDM3 of 8102
 nCODEC_EN,    // Chip select to CODEC device
 nBOOTPh,nBOOTPs;    // Boot Sector protection for Flashes
output      HEE0_Out;   // EE0 for Host
output      SEE0_Out;   // EE0 for Slave
output      nDBUFXEN,   // Enable for on-board periperals buffer
            nDBUFBEN;   // Enable for off-board periperals buffer to access to another boards
output      nSTBUFEN;   // Enable for ext. buffer driven Board Configuration Identificator (BCONF[0:1])
                        // and Board Revision (BREVN[0:2]) when read from BCSR5
output [3:1] MODCKh_Out; // MODCK1-3 comming from DIP-switch for setting Host(8101) PLL mode
output [1:3] nHRST;      // Three HRESETs to external boards
//*** LEDs drive pins ***//
```

```
output      nLED_EN;    // Allow to switch off all LEDs on the ADS accordingly to TTM req.
output [0:1] SIGH_LED,    // Misc two LEDs for SW indication for Host
            SIGS_LED;   // Misc two LEDs for SW indication for Slave
output  SEE1_LED;  // Slave in-Debug Mode indication
//*** Slave configuration pins ***//
output [0:2] BM_Out;      // Boot Mode selection three bits for the
output      n32to64En;   // Output for MUX control
output      CNFGS_Out,   // Configuration Source
            DSI64_Out,   // DSI 64bit setting
 DSISYNC_Out, // DSI Synchronous Mode
 SWTE_Out,  // Software Watchdog Timer Enable
 RSTCFG_Out,  // Reset Configuration Mode
 MODCK1s_Out, // Two lines of MODCK
 MODCK2s_Out;
`define CFGPINS
 {BM_Out[0:2],CNFGS_Out,DSI64_Out,DSISYNC_Out,SWTE_Out,RSTCFG_Out,MODCK1s_Out,MODCK2s_Out}
   // All the pins defined Slave PORESET configuration
//*** Test mode ***//
output TEST_EN;   // Enter 8102 to test mode
output [1:3] TEST_SIG;   // Select test mode
output      EE1_misc_Out;
//*** Registers Definition ***//
reg   [0:7] DataO;
//**** BCSR0 Description ****//
reg [0:7] BCSR0;
`define        FLASHPRT1  BCSR0[0] // Flash 1 H/W Protection
`define        FLASHPRT2  BCSR0[1] // Flash 2 H/W Protection
`define  FRM_RST   BCSR0[2] // Framer E1/T1 Reset contol
`define  CODEC_EN   BCSR0[3] // CODEC Chip Select
`define        SIGNALS0   BCSR0[4] // Signal-0 LED Slave
`define        SIGNALS1   BCSR0[5] // Signal-1 LED Slave
`define        SIGNALH0   BCSR0[6] // Signal-0 LED Host
`define        SIGNALH1   BCSR0[7] // Signal-1 LED Host
//**** BCSR1 Description ****//
reg [0:7] BCSR1;
`define        RECONF   BCSR1[0] // Start Slave Re-configuration
`define        HRST1   BCSR1[1] // Hard Reset to External Slave1
`define HRST2      BCSR1[2] // Hard Reset to External Slave2
`define ATM_RST   BCSR1[3] // ATM Framer Reset
`define HRST3      BCSR1[4] // Hard Reset to External Slave3
`define FETH_RST   BCSR1[5] // Fast Ethernet phy Reset
`define RS232EN_1  BCSR1[6] // RS232 Transceiver Host Side Enable
`define RS232EN_2  BCSR1[7] // UART Transceiver Slave Side Enable
//**** BCSR2 Description ****//
reg [0:7] BCSR2;
`define RSTCNF     BCSR2[0] // Reset Configuration Mode
`define        CNFG      BCSR2[1] // Configuration Source
`define SWTE    BCSR2[2] // Software Watchdog Timer Enable
`define DSI64      BCSR2[3] // System/DSI 64/32 bit
`define DSISYNC    BCSR2[4] // DSI Synchronous Mode
`define HRST       BCSR2[5] // Hard Reset to Slave
```

```
`define SRST      BCSR2[6] // Soft Reset to Slave
`define FRMtoTSI  BCSR2[7] // FALC56 connects to TSI or to TDM3 of 8102
//**** BCSR3 Description ****//
reg [0:7] BCSR3;
`define     CLKMD     BCSR3[0:1] // Clock Mode Setting Bits 1-2 for Slave
`define     SEE0   BCSR3[2]   // Slave Emulation Enable 0
`define      RSV34     BCSR3[3:4] // Reserved two bits
`define    BTMD      BCSR3[5:7] // Boot Mode for Slave Bits 0-2
//**** BCSR6 Description ****//
reg [0:7] BCSR6;
`define     FLUNLCK1   BCSR6[0]   // Flash 1 Protection Unlock
`define     FLUNLCK2   BCSR6[1]   // Flash 2 Protection Unlock
`define LEDEN     BCSR6[2]   // LED Enable| Hidden
`define     TEST      BCSR6[3]   // Test Mode Available|
`define    TESTSIG    BCSR6[4:6]  // Test Mode Select    | bits
`define     MARK      BCSR6[7]   // Mark Bit    |

reg      PRSTs;
reg      HEE0_Out;
reg      SEE0_Out;
reg      EE1misc_Out;

reg [divsee0:0] SEE0_count;
reg  NMIh,NMIs,HRESETh,SRESETh,HRESETs,SRESETs;
reg         clock_divider;
reg [divc:0]  counter;
reg [divd:0]  hhr,shr,nhr,hsr,ssr,nsr;

wire [1:0] CFG_ADDR = {A27,A28};
wire [2:0] BCSR_ADDR = {CFG_ADDR,A29};
wire READ_CFG_FROM_BCSR;
wire [0:7] CFG_BYTE3_DEF;
wire [0:7] BCSR4;
wire [5:7] BCSR5;      // Bits 0-4 are comming via ext. buffer
wire [0:3] SSEL;       // Address vector for Slaves Select
wire [0:3] ON_BRD_SLAVE_ADDR;
wire ON_BRD_HOST_PRPH;  // Active when select any of Host peripheral
wire OFF_BRD_SLAVE;     // Active when access to off-board Slave
wire Write_to_BCSR;
wire Read_from_BCSR;
wire [0:7] BCSR1r,BCSR2r;
wire [0:7] BCSR2_PON_DSI,BCSR2_PON_SYS;//BCSR3_PON;
wire [0:1] BCSR3_PONh;
wire [0:4] BCSR3_PONl;
wire [0:2] BTMD;
wire ADDR3,ADDR5;
wire WRITE3;
wire [1:10] CFGREG;
wire RESET_ACTIVE;
//*** Hard Reset Configuration Word (HRCW) ***//
parameter       EARB_DEF     = 1'b0,
```

```
                EXMC_DEF     = 1'b0,
                nIRQ7INT_DEF = 1'b1,
                EBM_DEF      = 1'b0,
                BPS_DEF      = 2'b10,
                SCDIS_DEF    = 1'b0,
                ISPS_DEF     = 1'b0,
              CFG_BYTE0_DEF  =     // 0x28
  {EARB_DEF,EXMC_DEF,nIRQ7INT_DEF,EBM_DEF,BPS_DEF,SCDIS_DEF,ISPS_DEF},
                IRPC_DEF     = 2'b00,
                DPPC_DEF     = 2'b00,
                NMIOUT_DEF   = 1'b0,
                ISB_DEF      = 3'b000,
              CFG_BYTE1_DEF  =     // 0x0
  {IRPC_DEF,DPPC_DEF,NMIOUT_DEF,ISB_DEF},
                RSV16_DEF    = 1'b0,
                BBD_DEF      = 1'b0,
                MMR_DEF = 2'b11,
                RSV20_21_DEF = 2'b00,
                TCPC_DEF     = 2'b10,
              CFG_BYTE2_DEF  =     // 0x02
  {RSV16_DEF,BBD_DEF, MMR_DEF,RSV20_21_DEF,TCPC_DEF},
                BC1PC_DEF    = 2'b00,
                RSV26_DEF    = 1'b0,
                DLLDIS_DEF   = 1'b0,
              // MODCK_H_DEF = 3'b100,
                RSV31_DEF    = 1'b0,
        CFG_BYTE3_0_3DEF  =     // 0x08
          {BC1PC_DEF,RSV26_DEF,DLLDIS_DEF},
           CFG_BYTE3_7DEF  = RSV31_DEF;
//*** Power-on-Reset value of BCSR0-3, BCSR6 ***//
parameter
         //*** BCSR0 PON value ***//
         FLASHPRT1_PON = 1'b0,
         FLASHPRT2_PON = 1'b0,
         FRM_RST_PON   = 1'b1,
         CODEC_EN_PON  = 1'b0,
  SIGNALS0_PON  = 1'b1,
         SIGNALS1_PON  = 1'b1,
         SIGNALH0_PON  = 1'b1,
         SIGNALH1_PON  = 1'b1,
  BCSR0_PON = {FLASHPRT1_PON, FLASHPRT2_PON,FRM_RST_PON,
   CODEC_EN_PON,SIGNALS0_PON,SIGNALS1_PON,
   SIGNALH0_PON,SIGNALH1_PON
  }, // 0x2f
         //*** BCSR1 PON value ***//
         RECONF_PON    = 1'b1,
         HRST1_PON     = 1'b1,
         HRST2_PON     = 1'b1,
         ATM_RST_PON   = 1'b1,
         HRST3_PON     = 1'b1,
         FETH_RST_PON  = 1'b1,
```

```
        RS232EN_1_PON = 1'b1,
        RS232EN_2_PON = 1'b1,
  BCSR1_PON =  {RECONF_PON,HRST1_PON,HRST2_PON,ATM_RST_PON,
HRST3_PON,FETH_RST_PON,RS232EN_1_PON,
RS232EN_2_PON
   },  // 0xff
  //*** BCSR2 PON value ***//
        RSTCNF_PON    = 1'b0,  // BCSR2.0
        DSISYN_PON    = 1'b0,  // BCSR2.4
  HRST_PON      = 1'b1,  // BCSR2.5
  SRST_PON    = 1'b1,  // BCSR2.6
  FRMtoTSI_PON  = 1'b1,  // BCSR2.7
        //*** BCSR3 PON value ***//
        RSV34_PON     = 2'b11,
  //*** BCSR6 PON value ***//
   FLUNLCK1_PON  =  1'b1,
        FLUNLCK2_PON  =  1'b1,
        LEDEN         =  1'b0,
        TEST          =  1'b0, // Disable Test Mode
        TESTSIG       =  3'b0,
        MARK          =  1'b0,
  BCSR6_PON =  {FLUNLCK1_PON, FLUNLCK2_PON, LEDEN, TEST,
                      TESTSIG, MARK}; // 0xd0

//*** Nodes ***//
assign READ_CFG_FROM_BCSR = (nCS0 == `ASSERTED) && (nHRESETh == `ASSERTED)
                           && (nFCFG == `From_BCSR) && !nW_R;
assign SSEL[0:3]         = {A7,A8,A9,A10};
assign ON_BRD_SLAVE_ADDR = GA[0:3]; // Apply 0xf for any out-of-CPCI backplane configuration
assign ON_BRD_HOST_PRPH  = !(nCS0 && nBCSR_CS && nATMCS);
assign OFF_BRD_SLAVE     = ((SSEL != ON_BRD_SLAVE_ADDR) && !nHCS1) || (!nHBCS && nW_R);
assign nDBUFBEN          = !(ON_BRD_HOST_PRPH || OFF_BRD_SLAVE);
     // to prevent contention on the Data bus to external boards
assign nDBUFXEN          = !OFF_BRD_SLAVE;
assign Write_to_BCSR  = /*!nPSDVAL && nW_R && */!nBCSR_CS;
assign Read_from_BCSR = !nW_R && !nBCSR_CS && nHRESETh;
assign BCSR2_PON_DSI  = {RSTCNF_PON,2'b10,nSYS64,DSISYN_PON,HRST_PON,SRST_PON,FRMtoTSI_PON};
assign BCSR2_PON_SYS  = {RSTCNF_PON,2'b01,nSYS64,DSISYN_PON,HRST_PON,SRST_PON,FRMtoTSI_PON};

assign BTMD           = DSItoSYS ? 3'b0 : 3'b001;
assign BCSR3_PONh  = {MODCK1s,MODCK2s};
assign BCSR3_PONl     = {RSV34_PON,BTMD};
assign BCSR4          = {SEE0_In,SEE1_In,SWOPT[0:2],3'b111};
assign BCSR5          = BCSR_ver;
assign ADDR3          = !A27 &&  A28 &&  A29;
assign ADDR5          =  A27 && !A28 &&  A29;
assign WRITE3         = Write_to_BCSR && ADDR3;
assign nSTBUFEN       = !(Read_from_BCSR && ADDR5);
assign BCSR1r[0:7]    = {`RECONF, nHRST_In[1:2],`ATM_RST,nHRST_In[3],`FETH_RST,`RS232EN_1,`RS232EN_2};
assign BCSR2r[0:7]    = {`RSTCNF,  `CNFG, `SWTE , nSYS64, `DSISYNC, nHRESETs, nSRESETs,`FRMtoTSI};
assign CFG_BYTE3_DEF  = {CFG_BYTE3_0_3DEF,MODCK4h,MODCK5h,MODCK6h,CFG_BYTE3_7DEF};
```

```
assign CFGREG[1:10]   = {`BTMD,`CNFG,`DSI64,`DSISYNC,`SWTE,`RSTCNF,MODCK1s,MODCK2s};
assign `CFGPINS       = (nPRSTs == `ASSERTED)? CFGREG[1:10] : 10'bz;
assign n32to64En      = !`DSI64;
//*** Outputs ***//
assign nLED_EN       = `LEDEN;
assign TEST_EN       = `TEST;
assign TEST_SIG[1:3] = (`TEST == `ACTIVE_HIGH)? `TESTSIG : 3'bz;
assign EE1_misc_Out  = EE1_misc_In; // temporary Null-Logic
assign MODCKh_Out    = (nHRESETh == `ASSERTED)? {MODCK3h,MODCK2h,MODCK1h} : 3'bz;
assign nFCSh         = (nFCFG == `From_FLASH)?  nCS0 : ((nHRESETh == `ASSERTED)? 1'b1 : nCS0);
assign FRMtoTSI      = `FRMtoTSI;
assign nBOOTPh       = ((`FLUNLCK1 == 1) && (`FLASHPRT1 == 0))? `ASSERTED : `NEGATED;
assign nBOOTPs       = ((`FLUNLCK2 == 1) && (`FLASHPRT2 == 0))? `ASSERTED : `NEGATED;
assign SIGH_LED[0]   = (`LEDEN == `ACTIVE_LOW)? ((nSRESETh == `ASSERTED)? `ASSERTED : `SIGNALH0):
`NEGATED;
                        // Also indicates SRESET assertion
assign SIGH_LED[1]   = (`LEDEN == `ACTIVE_LOW)? ((nHRESETh == `ASSERTED)? `ASSERTED : `SIGNALH1):
`NEGATED;
                        // Also indicates HRESET assertion
assign SIGS_LED[0]   = (`LEDEN == `ACTIVE_LOW)? ((nSRESETs == `ASSERTED)? `ASSERTED : `SIGNALS0):
`NEGATED;
                        // Also indicates SRESET assertion
assign SIGS_LED[1]   = (`LEDEN == `ACTIVE_LOW)? ((nHRESETs == `ASSERTED)? `ASSERTED : `SIGNALS1): `NE
GATED;
                        // Also indicates HRESET assertion
assign SEE1_LED      = (`LEDEN == `ACTIVE_LOW)? !SEE1_In : `NEGATED;
                        // Debug Acknowledge indication for the Slave
assign nCODEC_EN     = (`CODEC_EN  == `ACTIVE_LOW)? `ASSERTED : `NEGATED;
assign nRS232EN_1    = (`RS232EN_1 == `ACTIVE_LOW)? `ASSERTED : `NEGATED;
assign nRS232EN_2    = (`RS232EN_2 == `ACTIVE_LOW)? `ASSERTED : `NEGATED;
assign nFETH_RST     = (`FETH_RST == `ACTIVE_LOW)||(nHRESETh == `ASSERTED)? `ASSERTED : `NEGATED;
assign nATM_RST      = (`ATM_RST == `ACTIVE_LOW) ||(nHRESETh == `ASSERTED)? `ASSERTED : `NEGATED;
assign nFRM_RST      = (`FRM_RST == `ACTIVE_LOW) ||(nHRESETh == `ASSERTED)? `ASSERTED : `NEGATED;
assign HEE1_Out      = (HEE1_In == `ASSERTED)? HEE1_In : 1'bz;
assign nNMIh         = ( NMIh == `ASSERTED)? `ASSERTED : `NEGATED;
assign nNMIs         = ( NMIs == `ASSERTED)? `ASSERTED : 1'bz;
//***  Resets Output *** //
assign nHRESETh      = ( HRESETh == `ASSERTED)? `ASSERTED : 1'bz ;
assign nSRESETh      = ( SRESETh == `ASSERTED)? `ASSERTED : 1'bz ;
assign nSRESETs      = (`SRST == `ACTIVE_LOW || SRESETs == `ASSERTED)? `ASSERTED : 1'bz;
assign nHRESETs      = (`HRST == `ACTIVE_LOW || HRESETs == `ASSERTED)? `ASSERTED : 1'bz;
assign nPRSTs        = ((`RECONF == `ACTIVE_LOW) || (nHRESETh == `ASSERTED)) ? `ASSERTED : 1'bz;
assign nHRST[1]      = (`HRST1 == `ASSERTED)? `HRST1 : `NEGATED;
assign nHRST[2]      = (`HRST2 == `ASSERTED)? `HRST2 : `NEGATED;
assign nHRST[3]      = (`HRST3 == `ASSERTED)? `HRST3 : `NEGATED;
assign RESET_ACTIVE  = (reset == `ASSERTED) || (HRESETh == `ASSERTED);
//*** Execution Section ***//
//*** Generation Debug Request for Host ***//
always @ (posedge clk)
 begin
  HEE0_Out = HEE0_In;  // No extra logic - may be added in future
```

```
 end
//*** Synchronous Slave Soft Reset ***//
reg nSRESETs_d1,nSRESETs_d2,nSRESETs_d3;
always @ (posedge extclk)
 begin
  if(nSRESETs == `ASSERTED)    nSRESETs_d1 <= `ASSERTED;
  else     nSRESETs_d1 <= `NEGATED;
  if(nSRESETs_d1 == `ASSERTED) nSRESETs_d2 <= `ASSERTED;
  else    nSRESETs_d2 <= `NEGATED;
  if(nSRESETs_d2 == `ASSERTED) nSRESETs_d3 <= `ASSERTED;
  else    nSRESETs_d3 <= `NEGATED;
 end

//***  Slave Debug Request logic ***//
always @ (posedge extclk)
 begin
   if(nSRESETs_d3 == `ASSERTED)
    begin
     SEE0_count = 0;
 if (`SEE0 == `ASSERTED) SEE0_Out = 0;
 else      SEE0_Out = 1;
    end
   else begin
    if (WRITE3 && (Data[2] == 1)) begin
        SEE0_count = 0; SEE0_Out = 0;  // Produce short negage pulse
      end
    else begin
      if (SEE0_count[divsee0] != 1) begin
    SEE0_count = SEE0_count + 1; SEE0_Out = 0; // Activate Debug Request at rising edge
      end
  else SEE0_Out = !SEE0_In; // Permanent State of Debug Request pin
 end
   end
 end

//**** BCSR Register Main ****//
assign Data[0:7]      = DataO[0:7];
always @ (CFG_ADDR or READ_CFG_FROM_BCSR or BCSR_ADDR or Read_from_BCSR)
 if(READ_CFG_FROM_BCSR)
   case (CFG_ADDR)
     2'b00 :  DataO[0:7] = CFG_BYTE0_DEF;
 2'b01 :  DataO[0:7] = CFG_BYTE1_DEF;
 2'b10 :  DataO[0:7] = CFG_BYTE2_DEF;
 2'b11 :  DataO[0:7] = CFG_BYTE3_DEF;
   endcase
 else if(Read_from_BCSR)
   case (BCSR_ADDR)
     0 :  DataO[0:7] = BCSR0[0:7];
     1 :  DataO[0:7] = BCSR1r[0:7];
 2 :  DataO[0:7] = BCSR2r[0:7];
 3 :  DataO[0:7] = {BCSR3[0:1],SEE0_Out,BCSR3[3:7]};
```

```
 4 :  DataO[0:7] = BCSR4[0:7];
 5 :  DataO[0:7] = {5'bz,BCSR5[5:7]};
 6 :  DataO[0:7] = BCSR6[0:7];
   endcase
 else DataO[0:7] = 8'bz;

//**** BCSR Register Power-on-Reset setting & Write ****//

always @ (posedge nWE or negedge nHRESETh) // or negedge reset)
 begin
   if(nHRESETh == `ASSERTED)
 begin
   BCSR0[0:7] = BCSR0_PON; //  general
       BCSR1[0:7] = BCSR1_PON; //   board
       BCSR6[0:7] = BCSR6_PON; //  initialize
       {BCSR3[0:1],BCSR3[3:7]} = {BCSR3_PONh,BCSR3_PONl};
         if (!DSItoSYS) BCSR2[0:7] = BCSR2_PON_DSI;
     else           BCSR2[0:7] = BCSR2_PON_SYS;
 end
   else begin
      if (nHRESETs == `ASSERTED) `SEE0 = !SEE0_In; // Debug request to Slave
  if (Write_to_BCSR)
   case (BCSR_ADDR)
0: begin
    if(Data[0] == 1'b1)
     if(`FLUNLCK1  == `ASSERTED) `FLASHPRT1 = `NEGATED;
        else `FLASHPRT1 = `ASSERTED;
if(Data[1] == 1'b1)
                 if(`FLUNLCK2  == `ASSERTED) `FLASHPRT2 = `NEGATED;
    else `FLASHPRT2 = `ASSERTED;
                BCSR0[2:7] = Data[2:7];
    end
 1:  BCSR1[0:7] = Data[0:7];
 2:  {BCSR2[0:2],BCSR2[4:7]} = {Data[0:2],Data[4:7]};
 3:  BCSR3[0:7] = Data[0:7];
 6:  if (Data[7] == 1) BCSR6[0:6] = Data[0:6];
    endcase
end
 end

//**** Debounce functions ***//
function hhtime_elaps;
input i;
input [divd:0] d;
 begin
//   if (reset == `ASSERTED) begin hhtime_elaps = 1'bz; hhr = 1 << d; end
//   else begin
         if (i == 0) hhr = 0;
          else begin
                 if (hhr[d] != 1) begin
                    hhr = hhr + 1; hhtime_elaps = 1'b0;
```

```
            end else hhtime_elaps = 1'b1;
        end
//end
 end
endfunction

function shtime_elaps;
input i;
input [divd:0] d;
 begin
//  if (reset == `ASSERTED) begin shtime_elaps = 1'bz; shr = 1 << d; end
//  else
    if (i == 0) shr = 0;
    else begin
        if (shr[d] != 1) begin
            shr = shr + 1; shtime_elaps = 1'b0;
        end else shtime_elaps = 1'b1;
       end
 end
endfunction

function nhtime_elaps;
input i;
input [divd:0] d;
 begin
//   if (reset == `ASSERTED) begin nhtime_elaps = 1'bz; nhr = 1 << d; end
//   else
     if (i == 0) nhr = 0;
     else begin
         if (nhr[d] != 1) begin
             nhr = nhr + 1; nhtime_elaps = 1'b0;
         end else nhtime_elaps = 1'b1;
        end
 end
endfunction
function hstime_elaps;
input i;
input [divd:0] d;
 begin
//   if (reset == `ASSERTED) begin hstime_elaps = 1'bz; hsr = 1 << d; end
//   else
     if (i == 0) hsr = 0;
     else begin
         if (hsr[d] != 1) begin
             hsr = hsr + 1; hstime_elaps = 1'b0;
        end else hstime_elaps = 1'b1;
        end
   end
endfunction

function sstime_elaps;
```

```
input i;
input [divd:0] d;
 begin
//   if (reset == `ASSERTED) begin sstime_elaps = 1'bz; ssr = 1 << d; end
//   else
     if (i == 0) ssr = 0;
     else begin
           if (ssr[d] != 1) begin
              ssr = ssr + 1; sstime_elaps = 1'b0;
           end else sstime_elaps = 1'b1;
          end
 end
endfunction
function nstime_elaps;
input i;
input [divd:0] d;
 begin
//  if (reset == `NEGATED)
     if (i == 0) nsr = 0;
     else begin
           if (nsr[d] != 1) begin
               nsr = nsr + 1; nstime_elaps = 1'b0;
           end else nstime_elaps = 1'b1;
          end
 end
endfunction

//repeat(div1st) @(posedge clk);
always @ (posedge extclk)
 begin
   if (reset == `ASSERTED)
    begin
 counter = (1 << div1st) - 2;
// hhr = 1 << div2st; shr = 1 << div2st; hsr = 1 << div2st; /
// ssr = 1 << div2st; nhr = div2st << div2st; nsr = 1 << div2st;
end
   counter =  counter + 1;
   if (counter[div1st] != 1) clock_divider = 0;
   else                      clock_divider = 1;
 end
always @ (posedge clock_divider)
 begin
  if      (HReseth_In == `PRESSED) HRESETh = hhtime_elaps(0,div2st);
  else                             HRESETh = hhtime_elaps(1,div2st);
  if      (SReseth_In == `PRESSED) SRESETh = shtime_elaps(0,div2st);
  else                             SRESETh = shtime_elaps(1,div2st);
  if      (Aborth_In == `PRESSED)  NMIh = nhtime_elaps(0,div2st);
  else                             NMIh = nhtime_elaps(1,div2st);
 else                              NMIs = nstime_elaps(1,div2st);
 end
endmodule //BCSR_main
```

5.7 Schematics Drawing

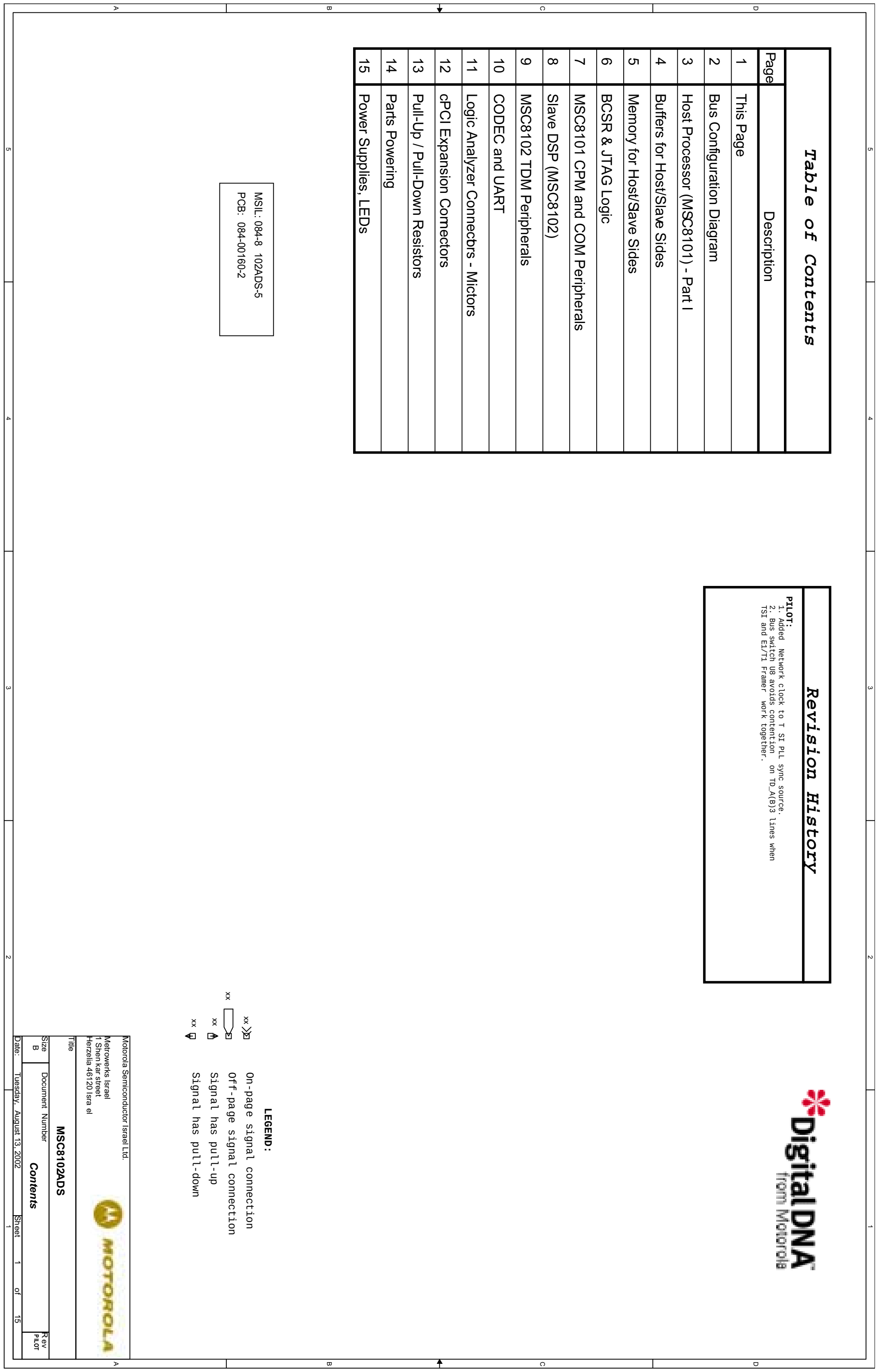


Figure 5-6 Schematics. Page 1

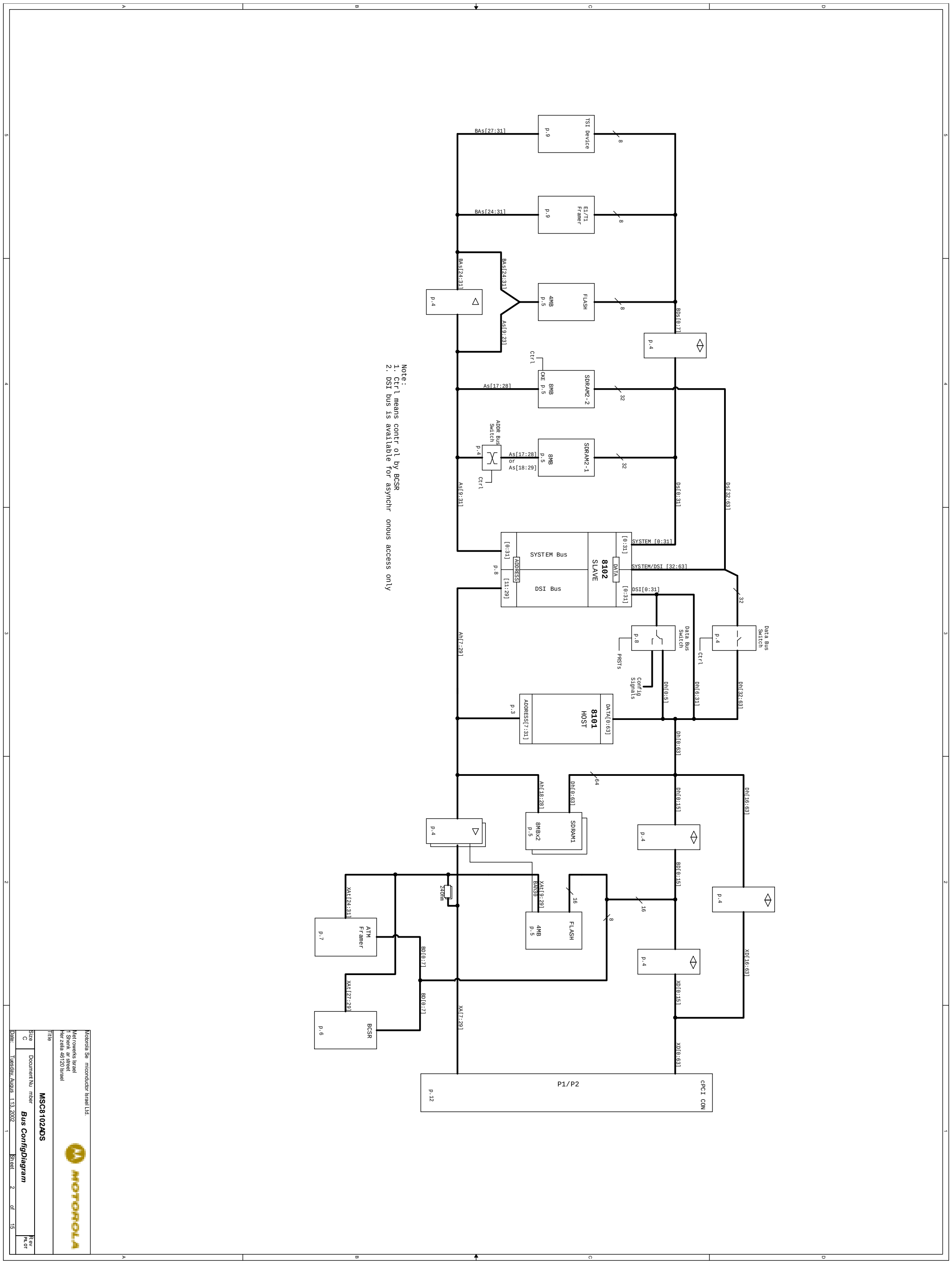


Figure 5-7 Schematics. Page 2

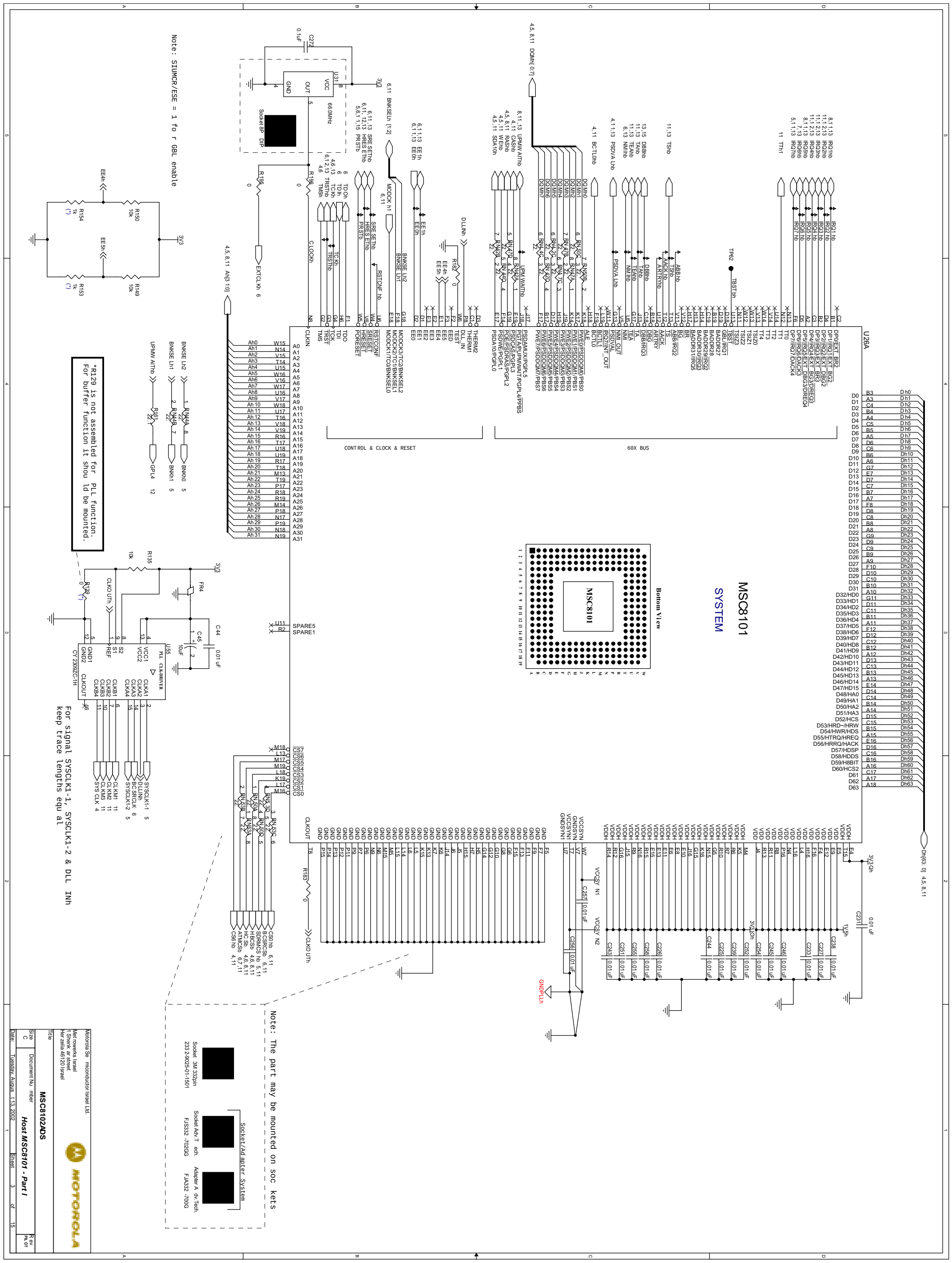
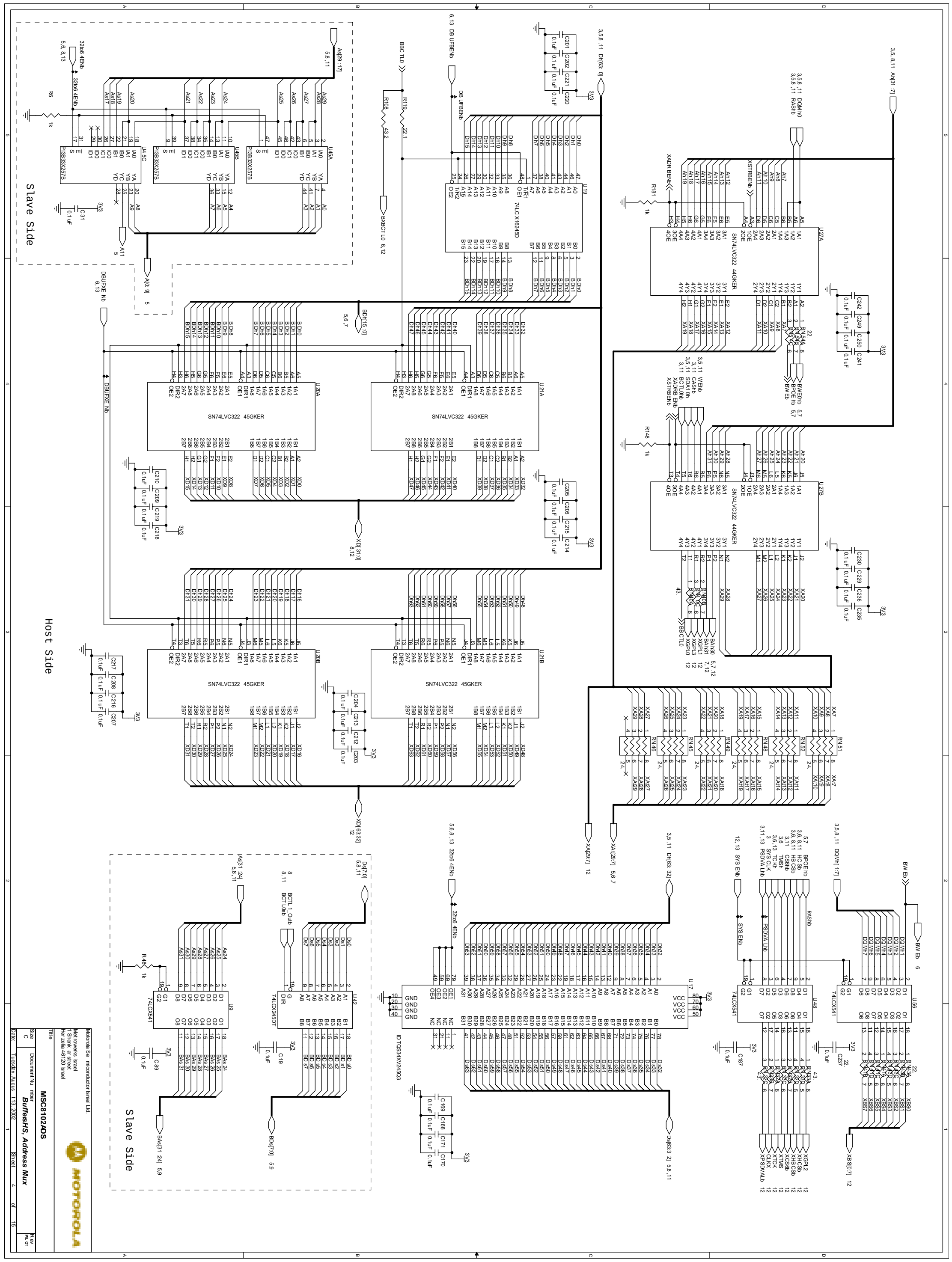


Figure 5-8 Schematics. Page 3



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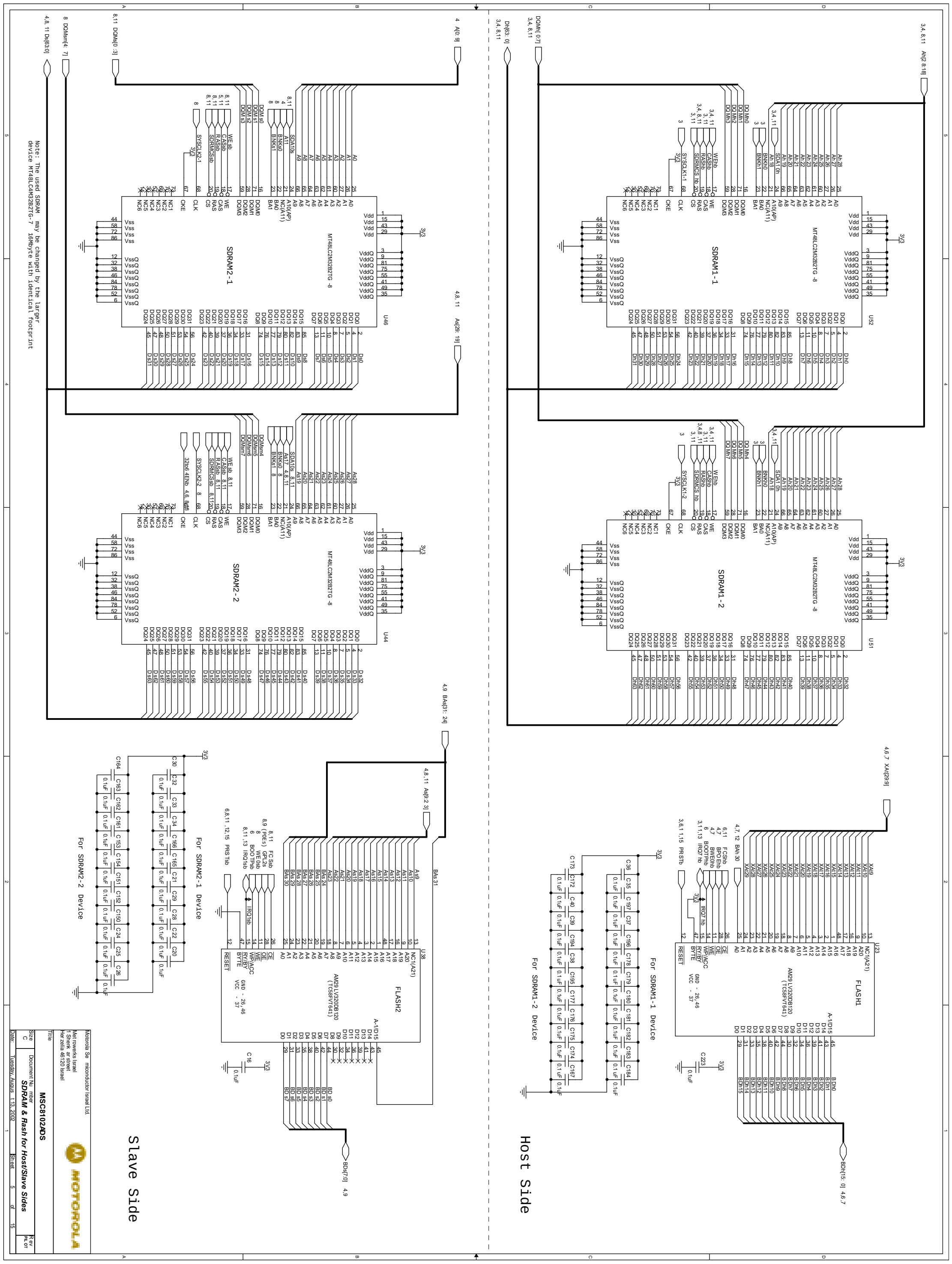

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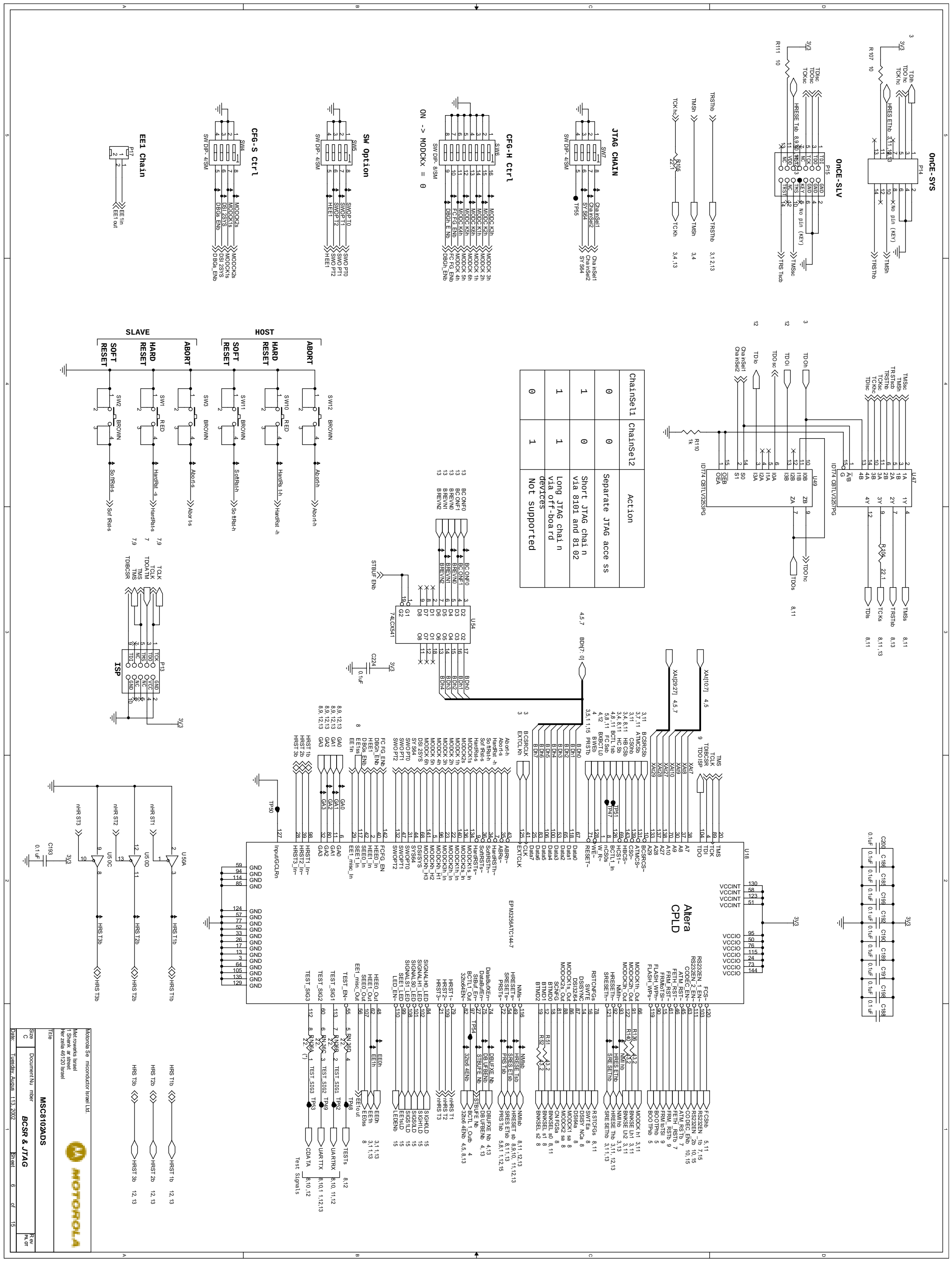

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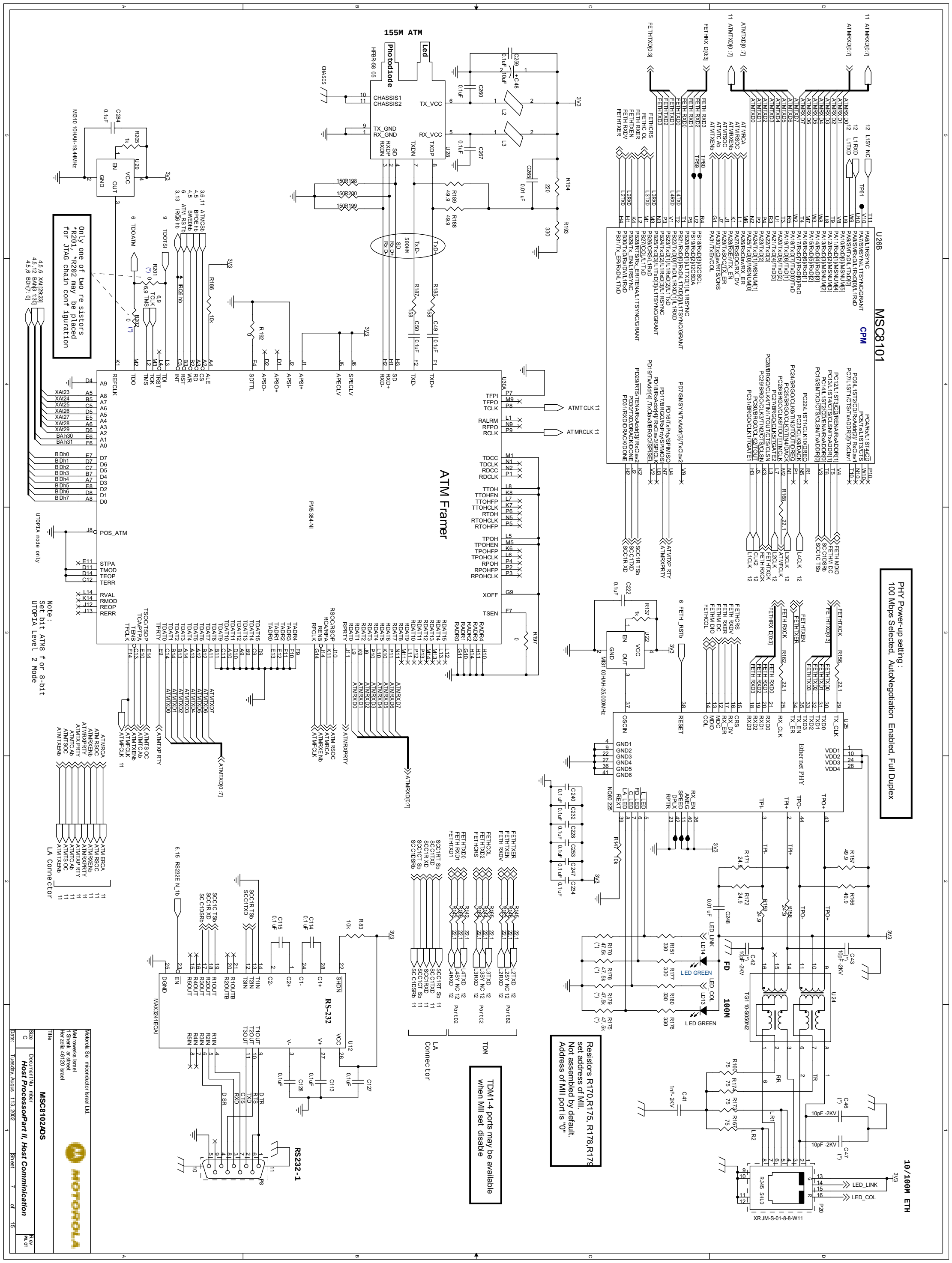

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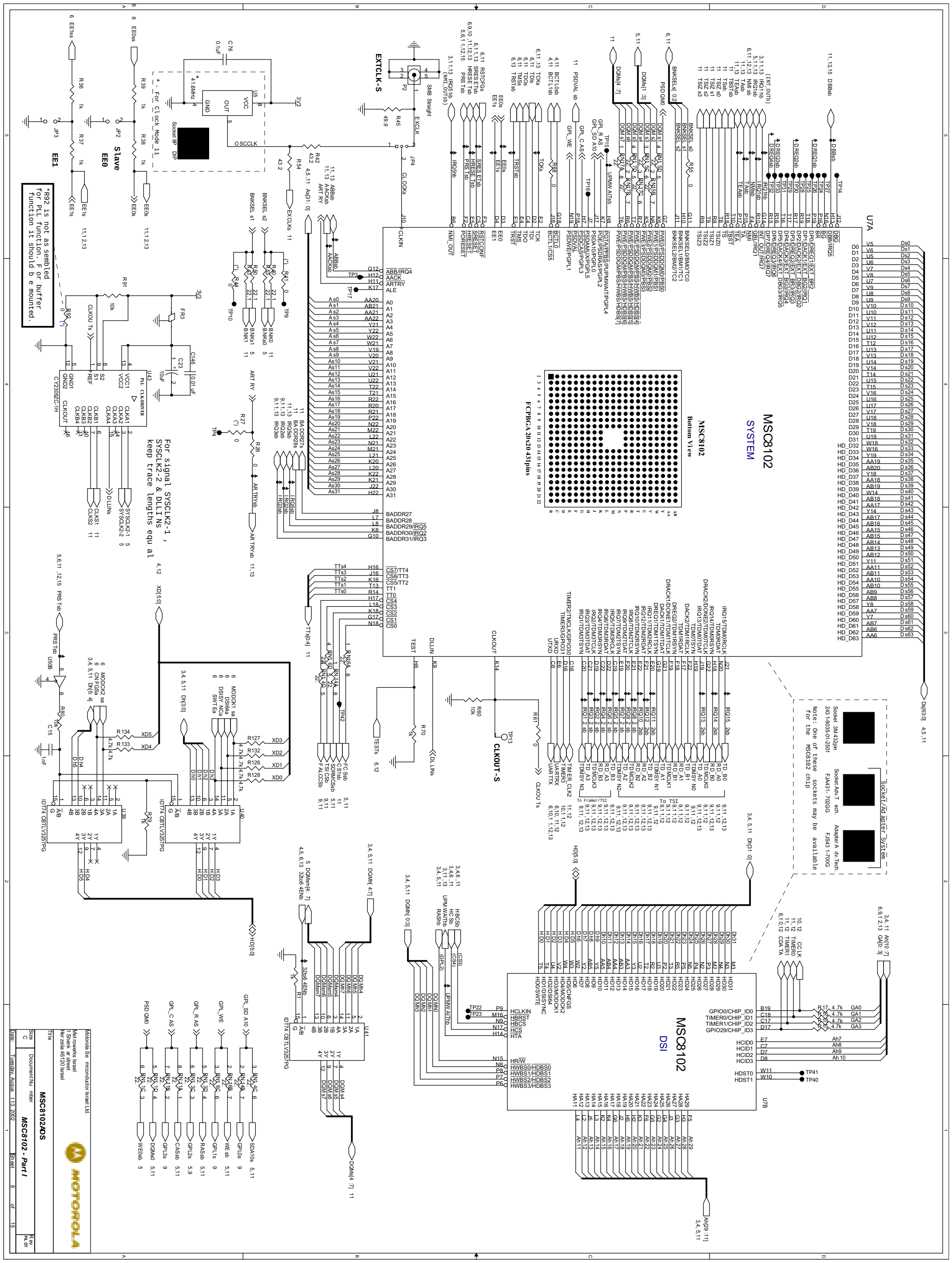

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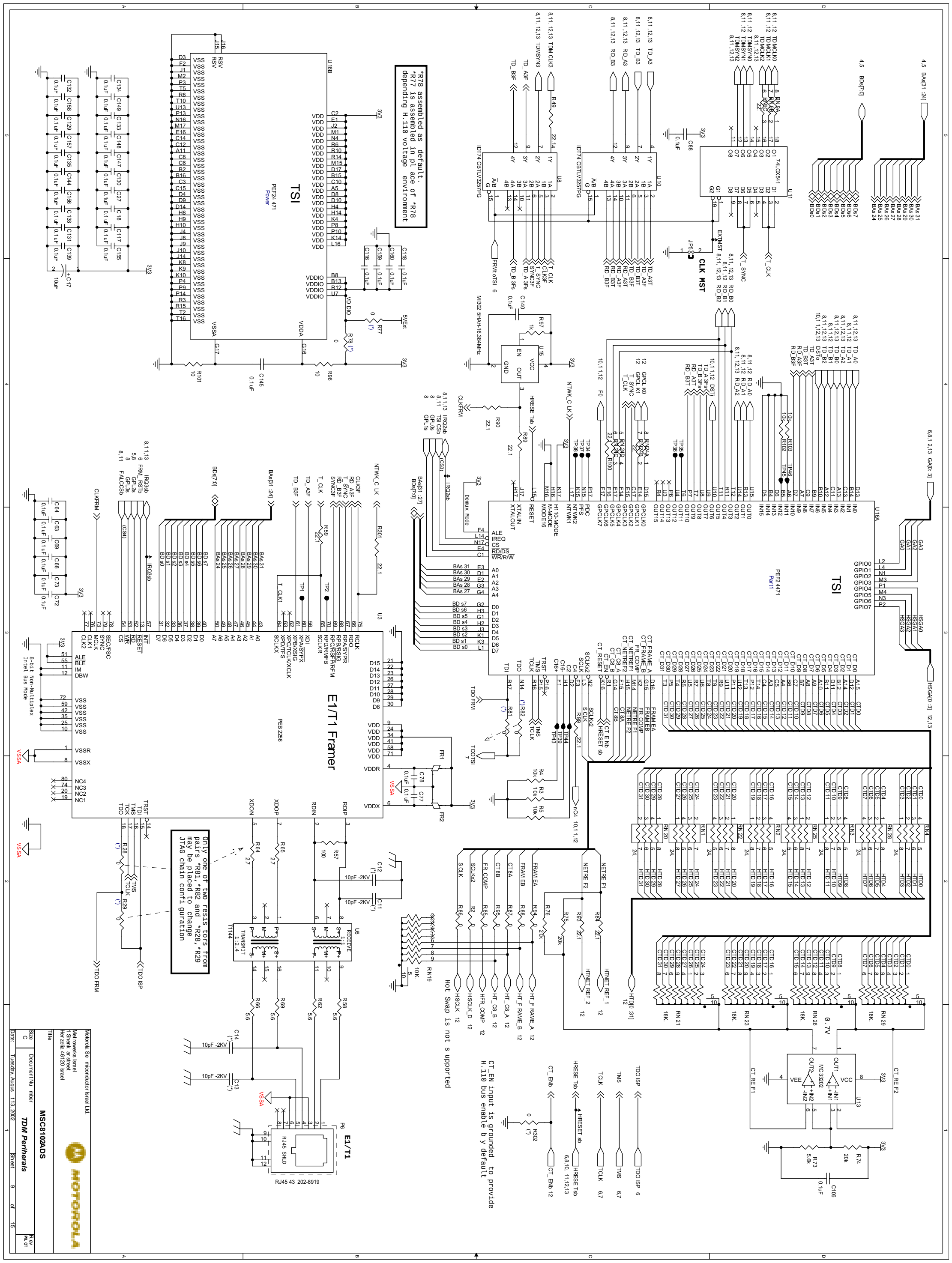

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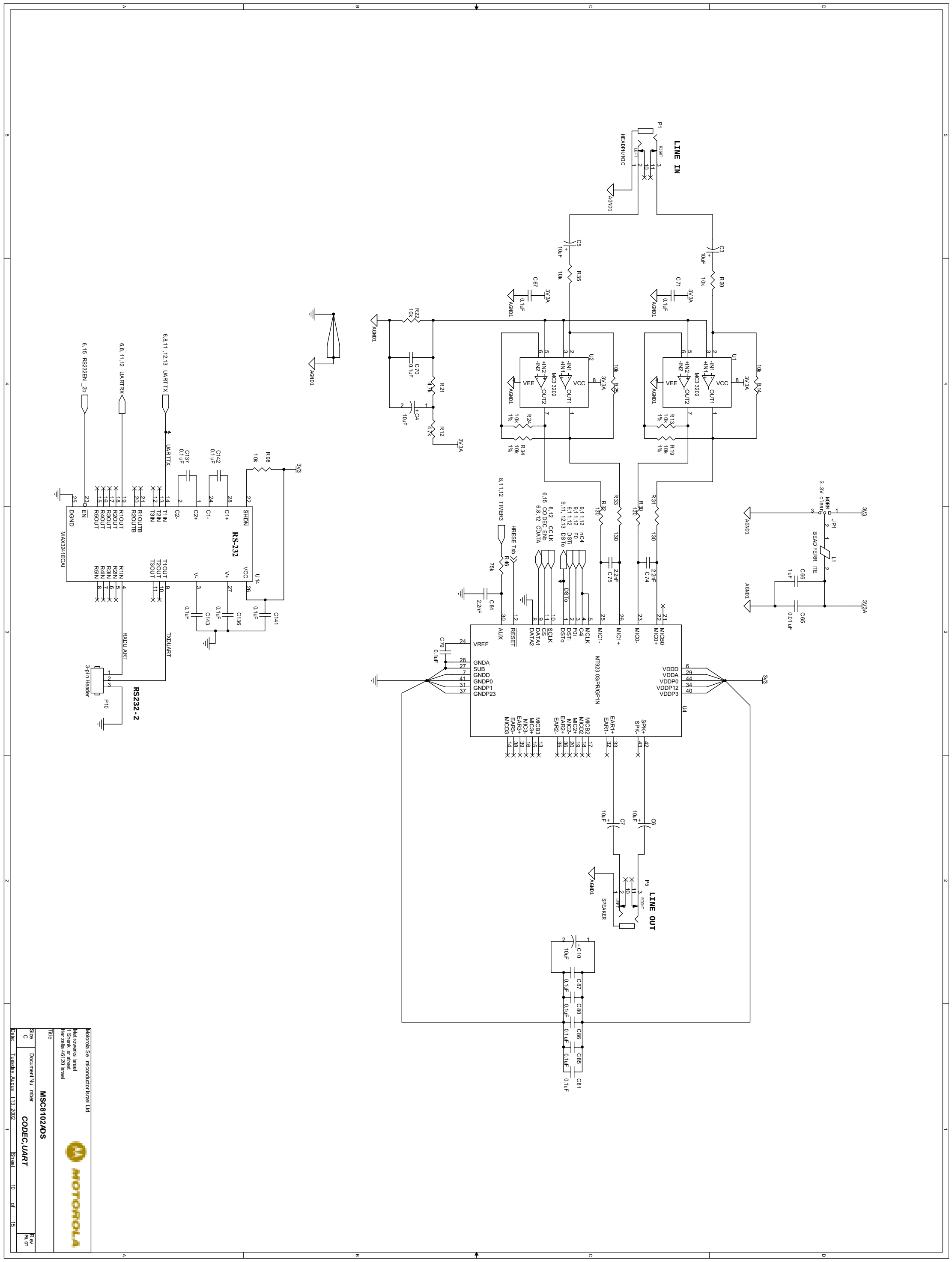

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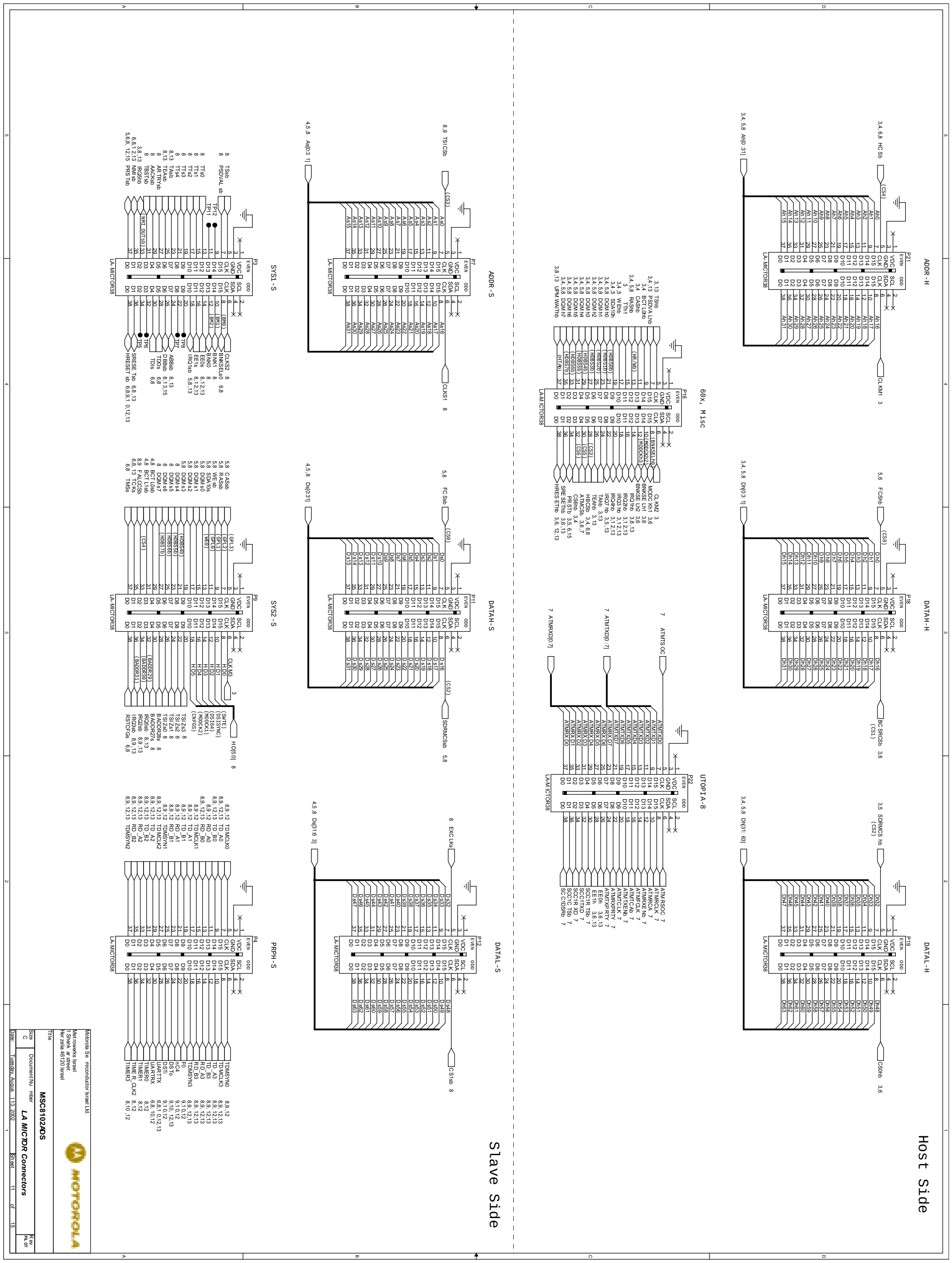

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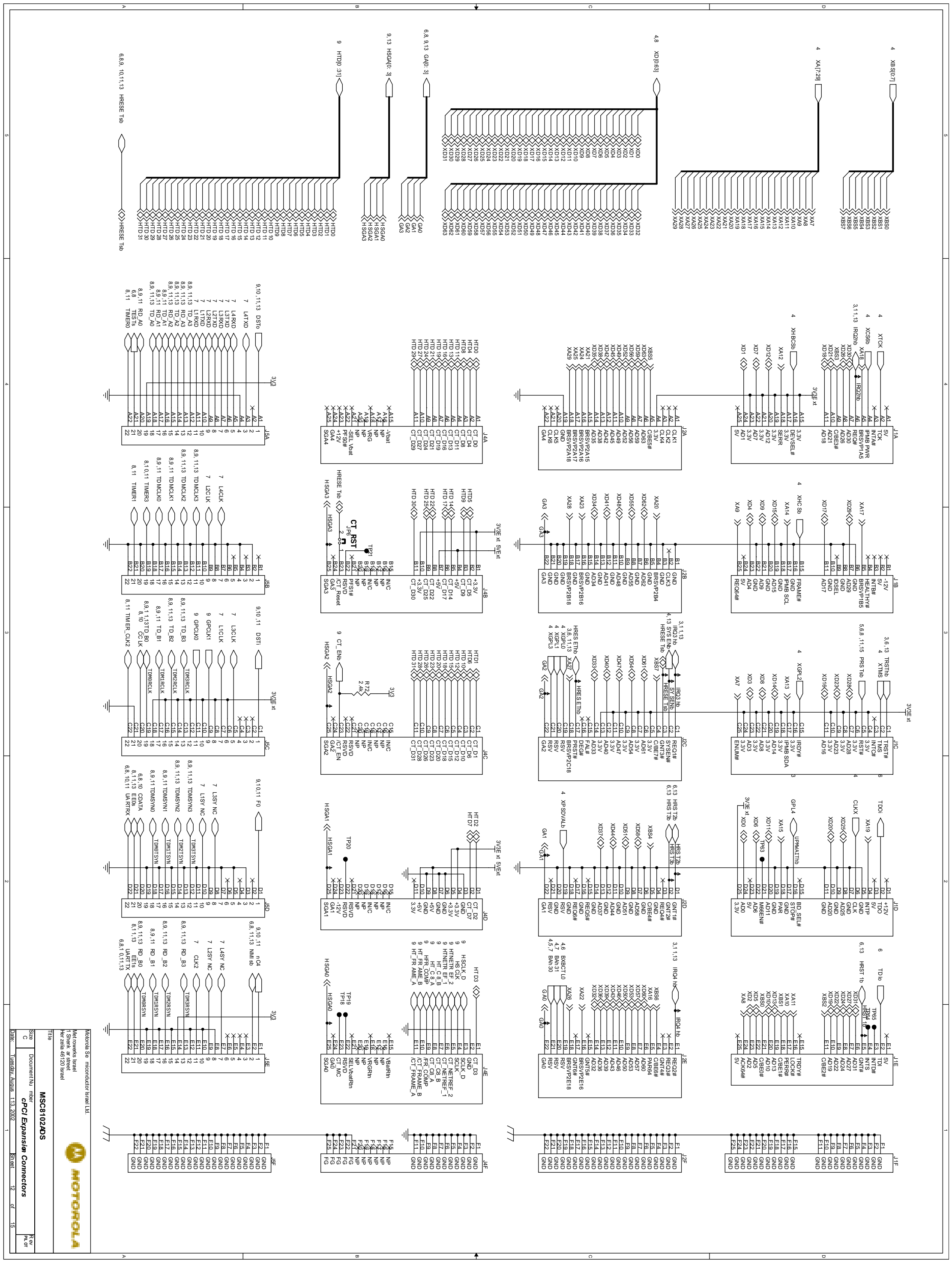

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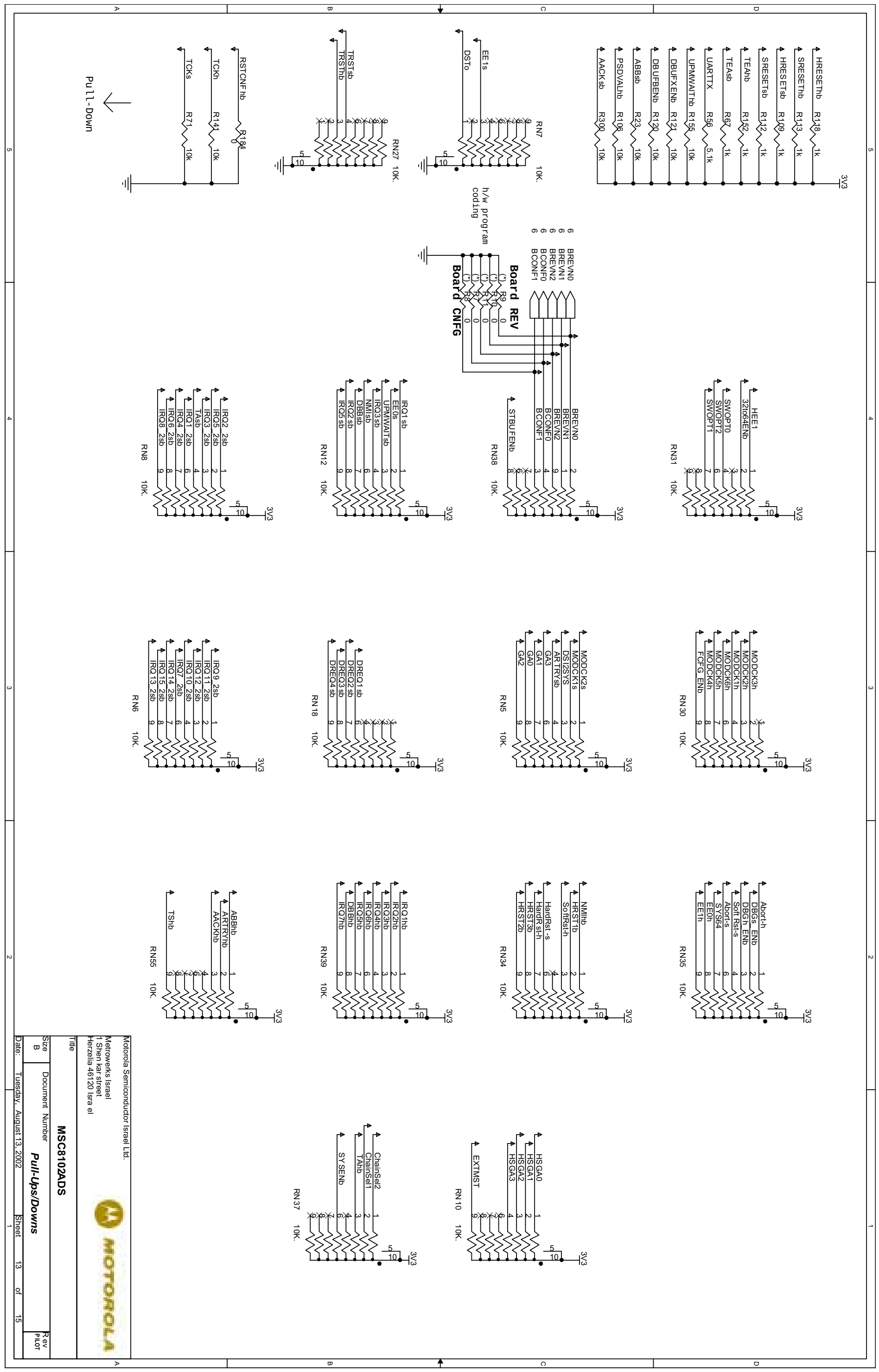

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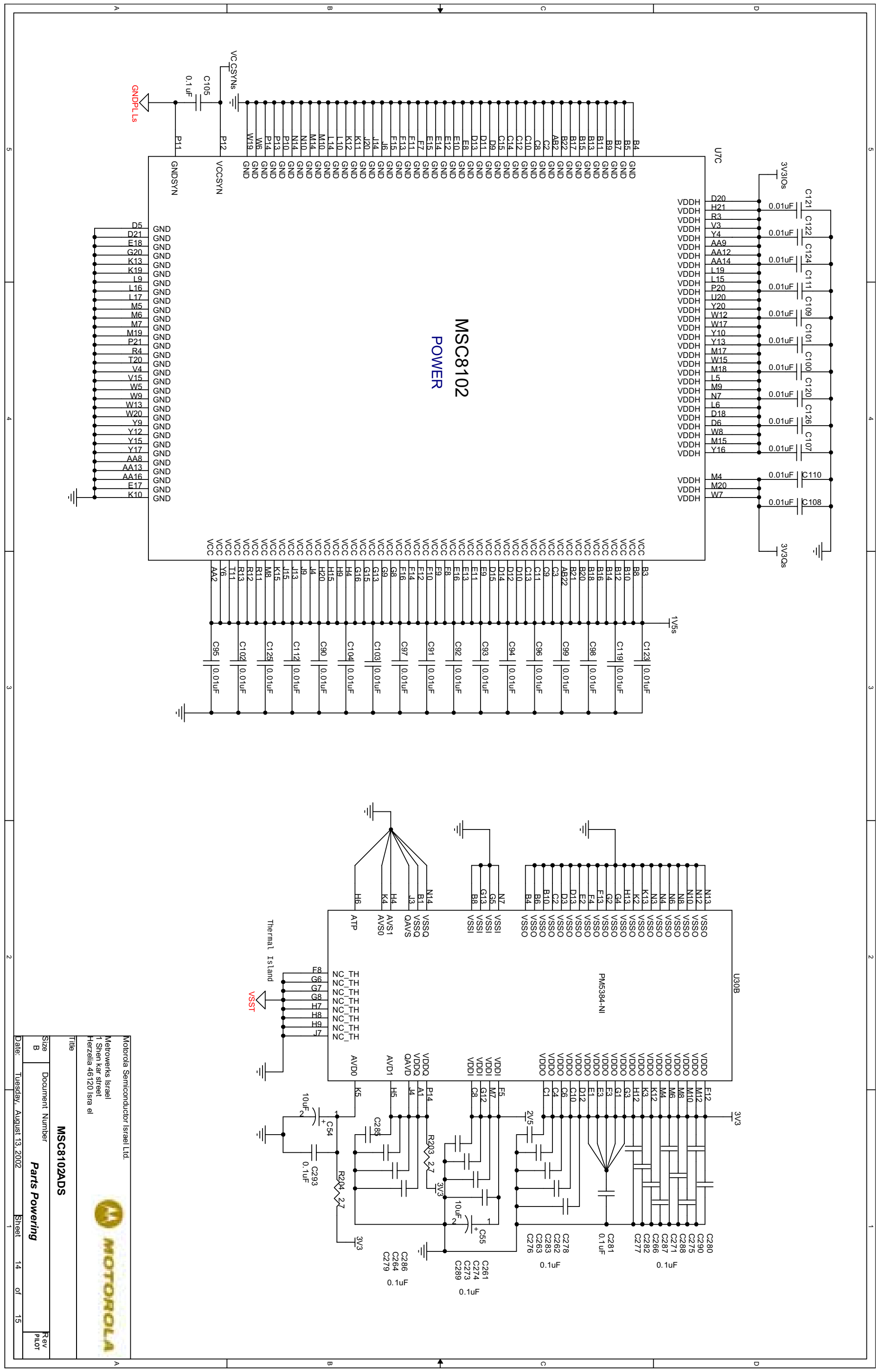

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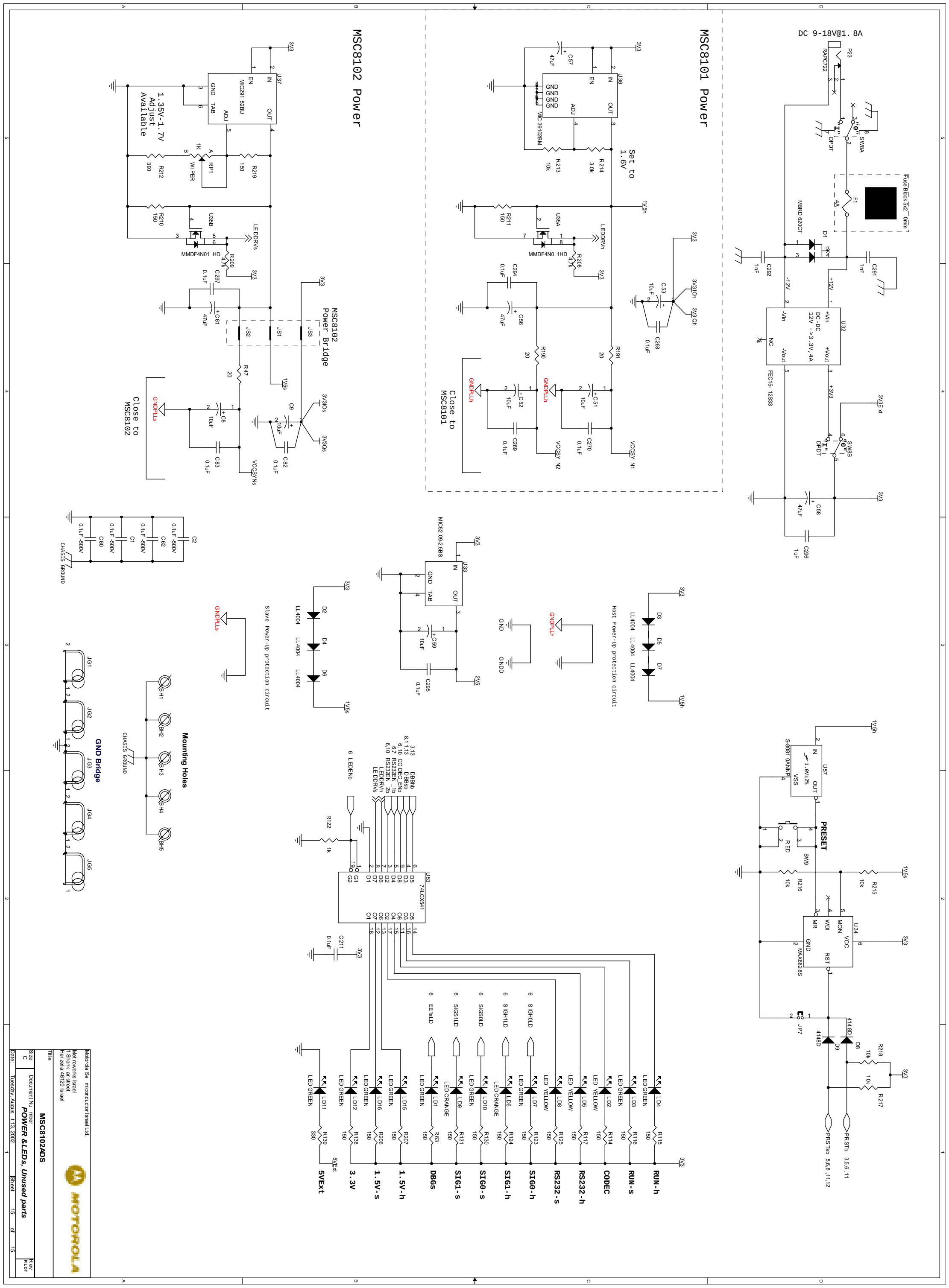

Figure 5-20 Schematics. Page 15

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